VLSI Laboratory

COURSE OBJECTIVES

- To educate students with the knowledge of verilog coding and test bench, to write verilog code for all logic gates, flip-flops, counters and adders etc.
- Students will be able to compile, simulate and synthesize the verilog code.
- From this lab the students will be able to draw the schematic diagram and layout for the inverter and amplifiers and verify their functionality.

COURSE OUTCOMES

- Write Verilog Code for the all logic gate circuits and their Test Bench for verification, observe the waveform and synthesize the code with the technological library, with the given Constraints.
- Write Verilog Code for the SR, JK, D, T flip-flop circuits and their Test Bench for verification, observe the waveform and synthesize the code with the technological library, with the given Constraints
- Write Verilog Code for the counters adder circuits and their Test Bench for verification, observe the waveform and synthesize the code with the technological library, with the given Constraints
- Design an Inverter with given specifications, completing the design flow mentioned below:

a. Draw the schematic and verify the following: i) DC Analysis ii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design

e. Verify & Optimize for Time, Power and Area to the given constraint

- Design the following circuits with the given specifications, completing the design flow mentioned below:

a. Draw the schematic and verify the following: i) DC Analysis ii) AC Analysis

iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design.

i) A Single Stage differential amplifier and op-amp

ii) Common source and Common Drain amplifier

VLSI Laboratory Tools