Scheme and Syllabus

of

M. Tech. ECE (VLSI)

(2022-2023 onwards)

Offered by:

Department of Electronics & Communication Engineering

NATIONAL INSTITUTE OF TECHNOLOGY DELHI

Delhi-110036

(An autonomous Institute under the aegis of Ministry of Education, Govt. of India)

Approved in the Board of Studies-Dept. of ECE held on March 1st, 2023.

Department of Electronics and Communications Engineering
National Institute of Technology Delhi

1.1 About the Department

Welcome to the Department of Electronic and Communication Engineering (ECE), National Institute of Technology Delhi. It was established in 2010, immediately with the beginning of the Institute under the aegis of the Ministry of Human Resource and Development (MHRD), Govt. of India. Currently, Department is offering one Undergraduate Program as B. Tech (ECE) and two Postgraduate programs as M. Tech. ECE and M. Tech. ECE (VLSI). The Department also offers Ph.D. and Post-Doctoral Fellowship (PDF) Programme in relevant areas. It has excellent laboratories and research facilities in electronic devices and circuits, electronic measurement and instrumentation, microprocessor and microcontroller, microwave and antenna design, optical fiber communication and optical device, multimedia, and advanced communication and VLSI design automation and simulation laboratory. The Department has received projects, grants, and fellowships from the Ministry of Electronics and Information Technology (MeitY), the Department of Science and Technology (DST)-SERB, and other funding agencies. The Department has active collaborations with academic & research institutes in India and abroad.

The Department of ECE has a blend of young as well as experienced dynamic faculty members and is committed to providing quality education and research in the field. Faculty members of the department have excellent academic & research credentials and published numerous peer-reviewed journal articles/ papers, Books, Book Chapters, etc. in the diversified field and have adequate experience in advanced research. The department of ECE provides a creative learning environment to the students for excellence in technical education. Here the students learn to face the challenges related to emerging technologies in electronics and communication engineering. The department of ECE promotes a self-learning attitude, entrepreneurial skills, and professional ethics. The department hopes to achieve the national goals and objectives of industrialization and self-reliance. As a result, it hopes to produce post graduates with strong academic and practical backgrounds so that they can fit into the academia, research and industry.

1.2 Vision

Create an educational environment to prepare the students to meet the challenges of the modern electronics and communication industry through state of art technical knowledge and innovative approaches beneficial to society.

1.3 Mission

- To promote teaching and learning by engaging in innovative research and by offering state-of-the-art undergraduate, postgraduate, and doctoral programs.
- To cultivate an entrepreneurial environment and industry interaction leading to the emergence of creators, innovators, and leaders.
- To promote co-curricular and extra-curricular activities for the overall personality development of the students.
- Building of responsible citizens through awareness and acceptance of ethical values.

M. Tech. ECE (VLSI)

2.1 Salient Features/ Philosophy of the M. Tech. ECE (VLSI) program

M. Tech. ECE (VLSI) program offered at NIT Delhi is designed to equip the students with a unique blend of skill sets that include:

- Strong theoretical and experimental foundation
- Predominantly experiment oriented approach with access to well-equipped and specialized laboratories, and supervised internship/ Thesis work.
- Hands-on technical training
- Life skills orientation
- Hard and soft skills
- Business perspective, along with emphasis on innovation and entrepreneurship

Some of the salient features of M. Tech ECE (VLSI) curriculum are as follows:

- Minimum Credits requirements for completion of M.Tech ECE (VLSI) program is 80.
- The Curriculum is based on the guidelines of National Education Policy (NEP) – 2020.
- The curriculum has embedded the Multi Exit/ Multi Entry in the M. Tech program.
- The curriculum is designed to meet the prevailing and ongoing industrial requirements.
- The curriculum includes Project based Education with adequate exposure for Thesis work.
- The curriculum is flexible and offers adequate Choice of Electives (Program Elective Courses).
- The curriculum inherits the Value based Education aims the Holistic Development of the students.
- The Curriculum offers Digital Pedagogy & Flipped Learning with adequate motivation for Entrepreneurship/ Start-ups.

Cardinal Mention

Students exiting after completing 1st Year will be awarded Post Graduate Diploma in ECE (VLSI) respectively. A minimum Credit requirement for Post Graduate Diploma is 40 Credits.

2.2 Program Educational Objectives (PEOs)

PEO-1	To be technically competent in the design, development, and implementation of VLSI circuits and systems to solve complex problems in the domain of electronics and communication.
PEO-2	Students shall be competent in adapting to new technologies as well as lead research in order to achieve excellence in their professional career.
PEO-3	Enfold the capability to expand horizons beyond engineering for creativity, innovation and entrepreneurship.
PEO-4	Acquire competence and ethics for social and environmental sustainability with a focus on the welfare of humankind.

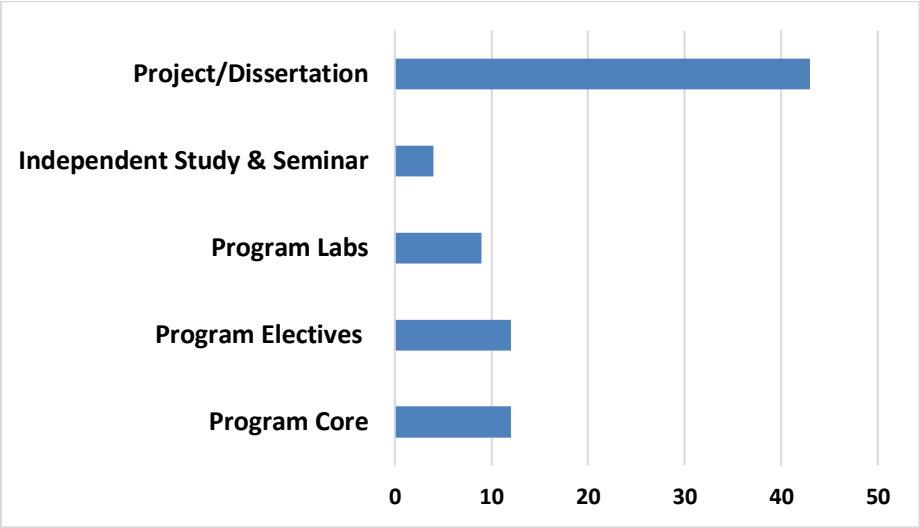
2.3 Program Outcomes (POs)

PO-1	Apply the knowledge of science, mathematics, and engineering principles for a problem-solving attitude and to acquire sound knowledge in the area of the VLSI domain.
PO-2	To design and analyze complex electronic circuits, using appropriate analytical methods as well as front-end and backend tools including prediction and modelling with an understanding of the limitations.
PO-3	An ability to independently carry out research /investigation and development work to solve practical problems and have the preparedness for lifelong learning.
PO-4	Ability to design and conduct experiments, as well as to analyse and interpret data, and synthesis of information.
PO-5	To comprehend and write effective reports and design documentation by adhering to appropriate standards and making effective presentations.
PO-6	Students will have a clear understanding of professional and ethical responsibility.

2.4 Program Specific Objectives (PSOs)

PSO -1	Enable students to get deep knowledge in the domain of VLSI Design and be able to solve complex problems in the field of Electronics and Communication Engineering.
PSO -2	Enable students to carry out research work in emerging technologies and to pursue career in higher studies and research.

3.1 Credit Distribution

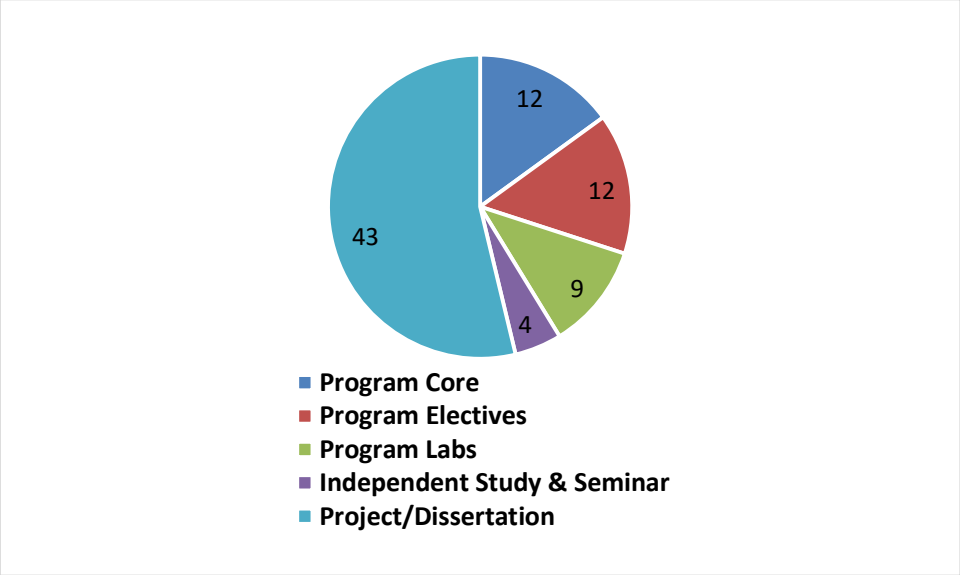


3.2 Semester wise Credit Structure

Credits						
S. No.	**Category of Courses**	**1st Year**		**2nd Year**		**Total**
		Semester I	**SemesterII**	**Semester III**	**Semester IV**	
1.	Program Core	9	3	-	-	**12**
2.	Program Electives	6	6	-	-	**12**
3.	Program Labs	3	6	-	-	**9**
4.	Independent Study & Seminar	2	2	-	-	**4**
5.	Project/Dissertation	-	3	20	20	**43**
Total		**20**	**20**	**20**	**20**	**80**

Minimum Credits Required for Award of Degree = 80

3.3 Credit Distribution (%)



Course Coding Pattern		
Semester	**M. Tech in ECE**	**M. Tech in ECE (VLSI)**
Departmental Core Courses (Theory)		
Autumn Semester	ECEM (5/6)0x (onwards)	ECVM (5/6)0x (onwards)
Spring Semester	ECEM (5/6)5x (onwards)	ECVM (5/6)5x (onwards)
Departmental Elective Courses (Theory)		
Autumn Semester	ECEM (5/6)2x (onwards)	ECVM (5/6)2x (onwards)
Spring Semester	ECEM (5/6)7x (onwards)	ECVM (5/6)7x (onwards)

Numeric for 1st year = 5; Numeric for 2nd year = 6;

Teaching SchemeforM. Tech ECE (VLSI)

Semester I					
Course Code	**Course Title**	**L**	**T**	**P**	**Credits**
ECVM 5xx	Core - I	3	-	-	3
ECVM 5xx	Core - II	3	-	-	3
ECVM 5xx	Core -III	3	-	-	3
ECVM 5xx	Elective-I	3	-	-	3
ECVM 5xx	Elective-II	3	-	-	3
ECVM 5xx	Lab - I	-	-	6	3
ECVM 507	Independent Study and Seminar	-	-	4	2
Total Credits		15	0	10	**20**

Semester II					
Course Code	**Course Title**	**L**	**T**	**P**	**Credits**
ECVM 5xx	Core IV	3	-	-	3
ECVM 5xx	Elective-III	3	-	-	3
ECVM 5xx	Elective-IV	3	-	-	3
ECVM 5xx	Lab - II	-	-	6	3
ECVM 5xx	Lab - III	-	-	6	3
ECVM 557	Independent Study and Seminar	-	-	4	2
ECVM 558	Minor Project	-	-	6	3
Total Credits		9	0	22	**20**

Semester III					
Course Code	**Course Title**	**L**	**T**	**P**	**Credits**
ECVM 601	Dissertation I	-	-	40	20
Total Credits					**20**

Semester IV					
Course Code	**Course Title**	**L**	**T**	**P**	**Credits**
ECVM 651	Dissertation II	-	-	40	20
Total Credits					**20**

List of Core Subjects

S. No.	Course Code	Course Title	L	T	P	Credits	Core Applicability
1.	ECVM 501	Semiconductor Devices	3	-	-	3	Core I + Core II + Core III
2.	ECVM 502	Digital IC Design	3	-	-	3	
3.	ECVM 503	Analog IC Design	3	-	-	3	
4.	ECVM 551	System-on-Programmable Chip Design	3	-	-	3	Core IV

List of Laboratory Subjects

S. No.	Course Code	Course Title	L	T	P	Credits	Lab Applicability
1.	ECVM 505	Analog and Digital Design Laboratory	-	-	6	3	Lab I
2.	ECVM 554	High level Design Laboratory	-	-	6	3	Lab II + Lab III
3.	ECVM 555	System-on-Programmable Chip Design Lab	-	-	6	3	

List of Elective Subjects

S. No.	Course Code	Course Title	L	T	P	Credits	Elective Applicability
1.	ECVM 520	Real Time Signal Processing Systems	3	-	-	3	Elective I + Elective II
2.	ECVM 521	VLSI Systems Design	3	-	-	3	
3.	ECVM 522	Embedded Systems & RTOS	3	-	-	3	
4.	ECVM 523	Architectural Design of IC`s	3	-	-	3	
5.	ECVM 524	VLSI Testing	3	-	-	3	
6.	ECVM 525	RF IC Design	3	-	-	3	
7.	ECVM 526	VLSI Technology	3	-	-	3	
8.	ECVM 527	VLSI Signal Processing	3	-	-	3	
9.	ECVM 528	Block chain Design and Use Cases	3	-	-	3	
10.	ECVM 570	Low Power Design Techniques	3	-	-	3	Elective III + Elective IV
11.	ECVM 571	Mapping Signal Processing Algorithm on DSP Architectures	3	-	-	3	
12.	ECVM 572	MOS Devices Modelling and Characterization	3	-	-	3	
13.	ECVM 573	Mixed Signal IC Design	3	-	-	3	
14.	ECVM 574	High Speed System (Board level) Design – (includes PCB design, thermal management, power supply)	3	-	-	3	

Curriculum in Detail (Core Courses)

Course Code	**ECVM 501**	**Semester: Odd (specify Odd/Even)**	**Semester : I Session: Autumn**
Course Name	**Semiconductor Devices**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To make the students understand the fundamentals of electronic devices and to train them to apply these devices in mostly used and important applications.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Basic Semiconductor Physics	Crystal lattice, energy band model, density of states, distribution statistics – Maxwell- Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, - drift, diffusion, thermionic emission, and tunnelling; excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger, radiative, and surface.

Unit II	Junctions	p-n junctions – fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristic, steady-state and transient conditions, capacitance model, reverse-bias breakdown, SPICE model; metal-semiconductor junctions – fabrication, Schottky barriers, rectifying ad ohmic contacts, I-V characteristics.
Unit III	MOS Capacitors and MOSFETs	The MOS capacitor – fabrication, surface charge –accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; the MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao-Sah and Schichman – Hodges models, I-V characteristic, second-order effects – Velocity saturation, short-channel effects, charge sharing model, hot-carrier effects, gate tunnelling; sub-threshold operation – drain induced barrier lowering (DIBL) effect, unified charge control model (UCCM), SPICE level 1, 2, and 3, and Berkeley short-channel IGFET model (BSIM).
Unit IV	MOSFETs and HEMTs	MESFETs –fabrication, basic operation, Shockley and velocity saturation models, I-V characteristics, high-frequency response, backgating effect, SPICE model; HEMTs – fabrication, modulation (delta) doping, analysis of III-V heterojunctions, charge control, I-V characteristics, SPICE model.
Unit V	BJPs and HBTs	BJTs – fabrication, basic operation, minority carrier distributions and terminal currents, I-V characteristic, switching, second-order effects – base narrowing, avalanche multiplication, high injection, emitter crowding, Kirk effect, etc.; breakdown, high-frequency response, Gummel Poon model, SPICE model; HBTs: - fabrication, basic operation, technological aspects, I-V characteristics, SPICE model.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Ben G. Streetman, Solid State Electronic Devices, Prentice Hall, 1997.
2.	Richard S. Muller and Theodore I. Kamins, Device Electronics for Integrated Circuits, John Wiley, 1986.
3.	S.M. Sze and Kwok K. Ng, Physics of Semiconductor Devices, 3rd edition, John-Wiley, 2006.
4.	Donald Neamen, An Introduction to Semiconductor Devices, McGraw-Hill Education, 2005.

Course Code	**ECVM 502**	**Semester: Odd (specify Odd/Even)**	**Semester : I Session: Autumn**
Course Name	**Digital IC Design**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To introduce the transistor level design of all digital building blocks common to all CMOS microprocessors, network processors, digital backend of all wireless systems etc., • To learn all important issues related to size, speed and power consumption.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	MOS Transistor Principles and CMOS Inverter	MOSFETcharacteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.
Unit II	Combinational Logic Circuits	Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.
Unit III	Sequential Logic Circuits	Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non Bistable Sequential Circuits.
Unit IV	Arithmetic Building Blocks	Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs
Unit V	Memory Architectures	Memory Architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Jan Rabaey, AnanthaChandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2.	N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design", Addision Wesley, 2nd Edition, 1993
3.	K.Martin - Digital integrated circuit design
4.	J.Kuo and J.Lou - Low voltage CMOS VLSI circuits
5.	M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
6.	Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill, 1998.

Course Code	**ECVM 503**	**Semester: Odd (specify Odd/Even)**	**Semester : I Session: Autumn**
Course Name	**Analog IC Design**		
Credits	**3**	**Contact Hours**	3
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To acquaint the students with basic CMOS analog building blocks and sub-system design. • To develop the ability to design and analyze MOS based Analog VLSI circuits to draw the equivalent circuits of MOS based Analog VLSI and analyze their performance.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Introduction	Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.
Unit II	Current Mirrors, Current and Voltage Reference	Basic current mirrors, cascode current mirrors, active current mirrors, low current biasing, supply insensitive biasing, temperature insensitive biasing, impact of device mismatch.
Unit III	Frequency Response of Amplifiers	Miller effect, CS amplifier, source follower, CG amplifier, cascade stage, differential amplifier, Multistage amplifier.
Unit IV	Operational Amplifiers	Performance parameters, One-stage and two stage Op Amps, gain boosting, comparison, common mode feedback, input range, slew rate, power supply rejection, noise in Op Amps, Buffered Op-amps, High speed/Frequency Op-amps
Unit V	Feedback Amplifiers	General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation
Course Assessmet	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition 2016.
2.	Paul. R.Gray and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.
3.	R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.
4.	T. C. Carusone, D. A. Johns and K. Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012
5.	P.E.Allen and D.R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.

Course Code	ECVM 503	Semester: Odd (specify Odd/Even)	Semester : I Session: Autumn
Course Name	System-on-programmable Chip Design		
Credits	3	Contact Hours	3
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	• To introduce the overall System on Chip (SoC) Design flow. • To introduce the System-level Design from processor selection to interconnection of all the modules and testing methods.		

Module No.	Title of the Module	List of Topics
Unit I	System-level Design	Driving Forces for SoC - Components of SoC - Design flow of SoC -Hardware/Software nature of SoC - Design Trade-offs - SoC Applications, Processor selection-Concepts in Processor Architecture: Instruction set architecture (ISA), Elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom-Designed processors- on-chip memory.
Unit II	Interconnection	On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, CoreConnect, Wishbone, Avalon - Network-on-chip: Architecture-topologies-switching strategies - routing algorithms -low control, Quality-of-Service-Reconfigurability in communication architectures.
Unit III	IP based system design	Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse - IP integration - IP evaluation on FPGA prototypes.
Unit IV	SOC Implementation	Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design.
Unit V	SOC Testing	Manufacturing test of SoC: Core layer, system layer, application layer- P1500 Wrapper Standardization-SoC Test Automation (STAT).
Course Assessme	Continuous Evaluation 25% Mid Semester 25% End Semester 50%.	

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Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Michael J.Flynn, Wayne Luk, "Computer system Design: Systemon-Chip", Wiley-India, 2012
2.	SudeepPasricha, NikilDutt, "On Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
3.	W.H.Wolf, "Computers as Components: Principles of Embedded Computing System Design",Elsevier, 2008.
4.	Patrick Schaumont "A Practical Introduction to Hardware/Software Co-design", 2nd Edition, Springer, 2012.
5.	Wayne Wolf, "Modern VLSI Design: IP Based Design", Prentice-Hall India, Fourth edition, 2009.

Syllabus in Detail (Laboratory Courses)

<table>
<tr><td>Course Code</td><td>ECVM 505</td><td>Semester: ODD (specify Odd/Even)</td><td colspan="2">Semester: I Session: Autumn
Month from: July to Dec</td></tr>
<tr><td>Course Name</td><td colspan="4">Design Laboratory (Digital and Analog)</td></tr>
<tr><td>Credits</td><td colspan="2">5</td><td>Contact Hours</td><td>6</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="3"></td></tr>
<tr><td>Teacher(s) (Alphabetically)</td><td colspan="3"></td></tr>
<tr><td>Course Objectives</td><td colspan="4">• To learn the fundamental principles of VLSI circuit design in digital and analog domain.
• To provide the exposure in high end hardware tools and technologies.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="3">List of Topics</td></tr>
<tr><td colspan="2" rowspan="3"></td><td colspan="3">I Digital Experiments (Based on Cadence)
• Study and analysis of the CMOS Inverter circuits.
• Study and analysis of Basing Gates in all type of Static logics.
• Study and analysis of Basing Gates in all type of Dynamic logics.
• Implementation of given Boolean expression in various logics and its analysis.
• Combinational and Sequential logic circuits design implementation.</td></tr>
<tr><td colspan="3">II Analog / IC Design Experiments (Based on Cadence/Any other equivalent SPICE Circuit Simulator and FPAA based experiments)
• Design and simulation of a simple five transistor differential amplifier – Measure gain, ICMR and CMRR.
• Layout generation, parasitic extraction and re-simulation of the five transistor differential amplifier.
• Analysis of results of static timing analysis.
• Design, Simulate and implement an inverting gain amplifier, low pass, high pass filters and full wave rectifier. Analyze the frequency response of filters.
• Design and Implement a circuit which introduces noise tone to the audio and then bring the original audio by removing the noise tone.</td></tr>
<tr><td colspan="3">Two case studies and one minor project.</td></tr>
<tr><td>Course</td><td colspan="4">Continuous Evaluation 50% End Semester 50%</td></tr>
</table>

Assessment	
Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	SPICE Manual
2.	IRSIM Manual
3.	MAGIC Manual
4.	Xilinx, Vivado Design Suite User Guide.
5.	Cadence Virtuoso Manual

Course Code	**ECVM 554**	**Semester: Even (specify Odd/Even)**	**Semester: II Session: Spring** Month from: January to May
Course Name	**High Level Design Laboratory**		
Credits	**3**	**Contact Hours**	6
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To learn the Hardware Description Language (Verilog/VHDL) • To provide hands on design experience with hardware/software based embedded system.		

Module No.	**Title of the Module**	**List of Topics**
		Experiments related to language semantics - Time Control: delay operator, event control. - Assignment Types: procedural, blocking, non-blocking, continuous. - Delay through combinational logic and nets • Behavioural Coding (examples and problems) • Structural Coding (examples and problems) • RT-Level Coding (examples and problems) • Mixed-Level Coding (examples and problems) • Coding of state machines and sequential logic • Coding of test benches • Coding style for synthesis
		Entering design constraints and synthesis using "FPGA Express" - Generating timing reports; CLB/gate usage reports; Identifying suitable FPGA device (Xilinx) for design implementation.
		Two case studies
		Minor project
Course Assessment	Continuous Evaluation 50% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	G. De Micheli, Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994.
2.	P. Kurup and T. Abbasi, Logic Synthesis Using Synopsys, Second Edition, Kluwer, 1996.

3.	J. Bhasker, A VHDL Primer, Third Edition, Prentice-Hall, 1999.
4.	Z. Navabi, Verilog Digital System Design, McGraw-Hill, 1999.
5.	S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice-Hall, 1996.

<table>
<tr><td>Course Code</td><td>ECVM 555</td><td>Semester: Even (specify Odd/Even)</td><td colspan="2">Semester: II Session : Spring
Month from: January to May</td></tr>
<tr><td>Course Name</td><td colspan="4">System-on-Programmable Chip Design Lab</td></tr>
<tr><td>Credits</td><td colspan="2">3</td><td>Contact Hours</td><td>6</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="3"></td></tr>
<tr><td>Teacher(s) (Alphabetically)</td><td colspan="3"></td></tr>
<tr><td>Course Objectives</td><td colspan="4">• To Design and develop complete hardware/software systems on an FPGA
• Efficiently break down complex computational tasks into hardware and software components, and build co-processor components for an FPGA-based processor.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="3">List of Topics</td></tr>
<tr><td colspan="2" rowspan="3"></td><td colspan="3">Can be designed around either Xilinx MicroBlaze / Altera NIOS / OpenRISC + Wishbone.
- Implementation of basic SoPC using tools.
- Interfacing with peripherals.
- Creation of custom peripherals using HDL.
- Enhancement of instruction.
- Set with custom instructions.
- Optimizing system architecture through choice of processor enhancements – architecture exploration</td></tr>
<tr><td colspan="3">Two case studies</td></tr>
<tr><td colspan="3">Minor project</td></tr>
<tr><td>Course Assessment</td><td colspan="4">Lab: Continuous Evaluation 50% End Semester 50%</td></tr>
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Syllabus in Detail (Elective Courses)

Course Code	**ECVM 520**	**Semester: Odd (specify Odd/Even)**	**Semester : Session:**
Course Name	**Real-time Signal Processing Systems**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To introduce efficient computation method of discrete Fourier transform for the real-time applications, and apply the signal processing algorithms for a wide range of real-time applications.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	The Discrete Fourier Transforms	Discrete Fourier transform, properties of DFT. Frequency domain sampling, Frequency analysis of signals using the DFT. DFT of discrete time signals, Relation between DFT and Z-transform. IDFT.
Unit II	Fast Fourier Transforms	Direct computation of DFT, Need of efficient computation of DFT, Radix-2 Decimation in time domain and decimation in frequency domain algorithms (DIT-FFT and DIF-FFT), Linear filtering methods based on DFT Goertzel Algorithms.
Unit III	Implementation of Discrete time systems	FIR Systems- Direct Form-I, Direct Form-II, Cascade, Parallel structure IIR Systems- Direct Form, Cascade, Linear phase structure, Frequency sampling structure
Unit IV	Design of IIR and FIR filters	Design of digital IIR digital filters from analog filters, Impulse invariance method and bilinear transformation method. Frequency transformations. Design of digital FIR filters using window method.
Unit V	Multirate DSP and Applications	Decimation and Interpolation, Multistage design of interpolators and decimators; Poly-phase decomposition and FIR structures, DSP device architecture and programming (TMS320C6x), Real-time system development, Code Composer Studio and DSP BIOS, Mini project (real-time application of DSP)
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%.	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	S. K. Mitra, "Digital Signal Processing: A Computer-Based Approach", Third edition, McGraw-Hill, 2006.

2.	J. Proakis, D. Manolakis, "Digital Signal Processing: Principles, Algorithms and Applications", Fourth edition, Prentice-Hall, 2006
3.	L.R. Rabiner and B. Gold, "Theory and Application of Digital Signal Processing", First edition, PHI Learning, 2008

Course Code	ECVM 521	Semester: (specify Odd/Even)	Session:
Course Name	VLSI System Design		
Credits	3	Contact Hours	3
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	• To introduce various aspects of VLSI circuits and their design including testing.		

Module No.	Title of the Module	List of Topics
Unit I	Introduction to VLSI Technology	VLSI design methodology, VLSI technology- NMOS, CMOS and BICMOS circuit fabrication. Layout design rules. Stick diagram. Latch up.
Unit II	MOS Characterization	Characteristics of MOS and CMOS switches. Implementation of logic circuits using MOS and CMOS technology, multiplexers and memory, MOS transistors, threshold voltage, MOS device design equations. MOS models, small-signal AC analysis. CMOS inverters, propagation delay of inverters, Pseudo NMOS, Dynamic CMOS logic circuits, power dissipation.
Unit III	Logic Synthesis	Programmable logic devices- Antifuse, EPROM and SRAM techniques. Programmable logic cells. Programmable inversion and expander logic. Computation of interconnect delay, Techniques for driving large off-chip capacitors, long lines, Computation of interconnect delays in FPGAs Implementation of PLD, EPROM, EEPROM, static and dynamic RAM in CMOS.
Unit IV	VLSI Design - Abstraction levels	Different abstraction levels in VLSI design; Design flow as a succession of translations among different abstraction levels; Gajski's Y-Chart; Need for manual designing to move to higher levels of abstraction with automatic translation at lower levels of abstraction; Need to model and validate the design at higher-levels of abstraction and the necessity of HDLs that encompass several levels of design abstraction in their scope.
Unit V	VLSI Testing	VLSI testing -need for testing, manufacturing test principles, design strategies for test, chip level and system level test techniques.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	M. Morris Mano and Michael D. Ciletti, 'Digital Design', Pearson, 5th Edition, 2013.
2.	Charles H. Roth, Jr, 'Fundamentals of Logic Design', Jaico Books, 4th Edition, 2002.
3.	William I. Fletcher, "An Engineering Approach to Digital Design", Prentice- Hall of India, 1980.

4.	Floyd T.L., "Digital Fundamentals", Charles E. Merril publishing company,1982.
5.	John. F. Wakerly, "Digital Design Principles and Practices", Pearson Education, 4 th Edition,2007.

Course Code	**ECVM 522**	**Semester: (specify Odd/Even)**	**Session :**
Course Name	**Embedded Systems & RTOS**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To enable the students to understand and use embedded computing platform. • To learn real time characteristics in embedded system design and explore system design techniques.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Embedded Processors	Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.
Unit II	Embedded Computing Platform	Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock.
Unit III	Networks	Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.
Unit IV	Real-Time Characteristics	Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.
Unit V	System Design Techniques	Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.
Course Assessment	Theory: Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers, 3rd edition, 2012.
2.	Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia, 2001.
3.	C. M. Krishna and K. G. Shin, "Real-Time Systems" , McGraw-Hill, 1997 .
4.	Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley & Sons, 2002.

Course Code	**ECVM 523**	**Semester: (specify Odd/Even)**	**Session:**
Course Name	**Architectural Design of IC's**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• This course covers algorithm, architecture and circuit design tradeoffs to optimize for power, performance and area.		

Module No.	Title of the Module	List of Topics
Unit I	Introduction	Introduction: VLSI Design flow, general design methodologies; Mapping algorithms into Architectures: Signal flow graph, data dependences, data path synthesis, control structures, critical path and worst case timing analysis, concept of hierarchical system design.
Unit II	Mapping algorithms into architectures	Data path element: Data path design philosophies, fast adder, multiplier, driver etc., data path optimization, application specific combinatorial and sequential circuit design, CORDIC unit;
Unit III	Pipeline and parallel architectures	Architecture for real time systems, latency and throughput related issues, clocking strategy, power conscious structures, array architectures;
Unit IV	Control strategies	Hardware implementation of various control Structures: micro programmed control techniques, VLIW architecture; Testable architecture: Controllability and Observability, boundary scan and other such techniques, identifying fault locations, self-reconfigurable fault tolerant structures;
Unit V	Issues in timing closure	Static and dynamic timing analysis, System considerations: edge triggered, clock skew, handling asynchronous inputs, sequential machines, clock cycle time, violation-maximum propagation delayrace through, Re-timings
Course Assessment	**Theory**: Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2nd edition, Oxford

	University Press, New York, 2010.
2.	M. D. Ercegovac and T. Lang, Digital Arithmetic, 1st edition, Elsevier, 2003.
3.	K. Ulrich, Advanced Arithmetic for the Digital Computer, Springer, 2002

Course Code	**ECVM 524**	**Semester: (specify Odd/Even)**	**Session:**
Course Name	**VLSI Testing**		
Credits	**4**	**Contact Hours**	**3**
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	• To study the Test Generation for Combinational and Sequential Circuits. • To study the Design for Testability and the Fault Diagnosis.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Introduction to Testing	Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault, error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits.
Unit II	Fault Models	Fault models, Fault Collapsing, Logic Simulation and Fault simulation, Fault simulation applications, General fault simulation algorithms-Serial, and parallel, Deductive fault simulation algorithms.
Unit III	Combinational circuit test generation	Combinational circuit test generation, Structural Vs Functional test, Path sensitization methods. Difference between combinational and sequential circuit testing, five and eight valued algebras, and Scan chain-based testing method.
Unit IV	Algorithms	D-algorithm procedure, Problems, PODEM Algorithm. Problems on PODEM Algorithm. FAN Algorithm. Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms
Unit V	Built in Self-Test (BIST)	Built in Self-Test (BIST) - Exhaustive pattern generation, random pattern generation, LFSR for pattern generation and Output response analysis, SISR, MISR, Memory BIST – Type of memory faults, fault detection by MARCH tests Issues in test and verification of complex chips, embedded cores and SOCs, System testing and test for SOCs.
Course Assessment	Theory: Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1. Bushnell Michael and Vishwani Agrawal, *Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*, Vol. 17, Springer Science & Business Media, 2004.

2.	Wang Laung-Terng, Cheng-Wen Wu, and Xiaoqing Wen, *VLSI test principles and architectures: design for testability*, Academic Press, 2006.
3.	AbramoviciMiron, M. A. Breuer and A. D. Friedman, *Digital Systems testing and testable design*, Computer Science Press, 1990.
4.	M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990.
5.	V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989

Course Code	**ECVM 525**	**Semester: (specify Odd/Even)**	**Session :**
Course Name	**RF IC Design**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To impart knowledge on basics of CMOS IC design at RF frequencies and to be familiar with the circuits used in RF front end in transceiver design.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Overview of RF Systems	Wireless Transmitter and Receiver Architecture – Heterodyne and SuperHeterodyne Systems - Basic concepts in RF design - units in RF Design, time variance - Effects of Nonlinearity: harmonic distortion, gain compression, cross modulation, intermodulation, cascaded nonlinear stages, AM/PM conversion - Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, representation of noise in circuits

Unit II	High frequency amplifier design	Types of amplifiers: Narrowband and Wideband Amplifiers - zeros as bandwidth enhancers, shunt-series amplifier, f T doublers, neutralization and unilateralization
Unit III	Need for LNA	Friis' equation - Low noise amplifier design – LNA topologies: noise cancelling LNA topology, distortion cancelling LNA topology - linearity and large signal performance
Unit IV	Need for Mixers	Noise and Linearity trade-off in RF Mixer design - traditional mixer circuits: multiplier-based mixers, subsampling mixers, diode-ring mixers - Noise Folding - Single-sideband and Double-sideband Noise Figure – Feedthrough: Single balanced and Double Balanced – IP3 and IP2 improvement - Oscillators and synthesizers – describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers – phase noise considerations
Unit V	RF power amplifiers	Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations. RFIC simulation and layout- General Layout Issues, Passive and Active
Course Assessment	**Theory**: Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	T.homas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", 2nd ed., Cambridge, UK: Cambridge University Press,2004.
2.	B.Razavi, "RF Microelectronics", 2nd Ed., Prentice Hall, 1998.
3.	A.A. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press,1999.
4.	R. Ludwig and P. Bretchko, "RF Circuit Design, Theory and Applications", Pearson,2000.
5.	Mattuck,A., "Introduction to Analysis", Prentice-Hall,1998.

Course Code	**ECVM 526**	**Semester: (specify Odd/Even)**	**Session:**
Course Name	**VLSI Technology**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To study the various techniques involved in the VLSI fabrication process.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Introduction to VLSI technology	Device scaling and Moore's law, basic device fabrication methods, alloy junction and planar process, Czochralski techniques, Characterization methods and wafer specifications, defects in Si and GaAs.
Unit II	Oxidation, Diffusion and ion-implantation	Types of oxidation and their kinematics, thin oxide growth models, stacking faults, oxidation systems, Deposition process and methods, Diffusion in solids, Diffusion equation and diffusion mechanisms, ion implantation technology, ion implant distributions, implantation damage and annealing, transient enhanced diffusion and rapid thermal processing
Unit III	Epitaxy and thin film deposition	Thermodynamics of vapor phase growth, MOCVD, MBE, CVD, reaction rate and mass transport limited depositions, APCVD/LPVD, equipments and applications of CVD, PECVD, and PVD.
Unit IV	Etching	Wet etching, selectivity, isotropy and etch bias, common wet etchants, orientation dependent etching effects; Introduction to plasma technology, plasma etch mechanisms, selectivity and profile control plasma etch chemistries for various films, plasma etch systems
Unit V	Lithography	Optical lithography contact/proximity and projection printing, resolution and depth of focus, resist processing methods and resolution enhancement, advanced lithography techniques for nanoscale pattering, immersion, EUV, electron, X-ray lithography.
Course Assessment	**Theory**: Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	James D. Plummer , "Silicon VLSI Technology: Fundamentals, Practice and Modelling", Pearson Education, 2000
2.	Sze, S.M., "VLSI Technology", 4th Ed., Tata McGraw-Hill, 1999
3.	C.Y. Chang and S.M.Sze, "ULSI Technology", McGraw Hill ,1996
4.	Gandhi, S. K., "VLSI Fabrication Principles: Silicon and Gallium Arsenide", John Wiley and Sons, 2003.
5.	Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", 2nd Edition, Oxford University Press 2001

Course Code	**ECVM 527**	**Semester: (specify Odd/Even)**	**Session :**
Course Name	**VLSI Signal Processing**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	• To introduce techniques for altering existing DSP structures to suit VLSI implementations.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Introduction to DSP Systems, Pipelining and Parallel Processing of FIR Filters	Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.
Unit II	Retiming, Algorithmic Strength Reduction	Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.
Unit III	Pipelining and Parallel Processing of IIR Filters	Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power- of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.
Unit IV	Bit-Level Arithmetic Architectures	Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters
Unit V	Synchronous, Wave and Asynchronous Pipelining	Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.
Course Assessme	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

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Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2.	U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2nd Edition, 2004.

Course Code	ECVM 528	Semester: (specify Odd/Even)	Session :
Course Name	Blockchain Design and Use Cases		
Credits	3	Contact Hours	3
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	• This course provides an overview of Blockchain and its application		

Module No.	Title of the Module	List of Topics
Unit I	Introduction	Blockchain Components and Concepts, Smart Contracts. Overview of the current financial system and its drawbacks. Advantages of Blockchain as an alternate financial system.
Unit II	Basics of cryptocurrencies	Cryptography, Hash Functions, Public Key Cryptography and Digital Signature.
Unit III	Bitcoin Fundamentals	Bitcoin's block structure, Consensus and mining processes in Bitcoin Bitcoin Trading, Scripting language in Bitcoin.
Unit IV	Permissioned Blockchain	Permissioned Blockchain Architecture, RAFT Consensus, Byzantine General Problem, Practical Byzantine Fault Tolerance.
Unit V	Application of Blockchain	Key Frameworks and Tools, Membership and Identity Management, Hyper ledger composer, Blockchain's implications on Traditional Business,Practical use-cases of Blockchain in Finance, Industry and Governance.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Melanie Swan, "Blockchain: Blueprint for a New Economy", O'Reilly Media, Inc., 2015
2.	Andreas M. Antonopoulos, "Mastering Bitcoin: Unlocking Digital Cryptocurrencies", Second Edition, O'Reilly Media, Inc., 2014

Course Code	ECVM 570	Semester: (specify Odd/Even)	Session :
Course Name	Low Power Design Techniques		
Credits	3	Contact Hours	3
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	• To understand probabilistic power analysis and circuit, logic level design, and analyze low power architectures& systems.		

Module No.	Title of the Module	List of Topics
Unit I	Introduction & Simulation power analysis	Need for low power VLSI chips, sources of power dissipation Device & technology impact on low power, impact of technology scaling, technology & device innovation, Power estimation, SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static power, gate level capacitance estimation, architecture level analysis, Monte-Carlo simulation
Unit II	Probabilistic power analysis & circuit level, logic level design	Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy, low power design, Power consumption in circuits, Flip-Flops & Latches design, high capacitance nodes, low power digital cells library, Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.
Unit III	Low power architecture & systems	Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design
Unit IV	Low power clock distribution	Power dissipation in clock distribution, single driver vs distributed buffers, zero skew vs tolerable skew, chip & package co-design technique of clock network.
Unit V	Algorithm & architectural level methodologies	Introduction, design flow, algorithmic level analysis & optimization, architectural level estimation & synthesis
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc.

(Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Kaushik Roy, Sharat Prasad, Low-Power CMOS VLSI Circuit Design, Wiley, 2000
2.	Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP, 2002
3.	Rabaey, Pedram, Low power design methodologies, Kluwer Academic, 1997

Course Code	**ECVM 571**	**Semester: (specify Odd/Even)**	**Session :**
Course Name	**Mapping Signal Processing Algorithms on DSP Architectures**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To analyze the algorithms, and mapping them to DSP architectures for certain kinds of operations. • To provide the fundamental bounds on performance, mapping to dedicated and custom resource shared architectures.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Introduction to DSP Systems and Algorithms	Digital systems, DSP, computer architecture, DSP computing algorithms, Direct Computing DFT, FFT, Gortzel.
Unit II	Firmware Development versus Architecture	Digital systems, DSP, computer architecture, DSP development platforms, C compiler, Impact of C on architecture and vice versa, Extensions to C, DSP-C, Simulation Technologies, program verification, Debug and emulation.
Unit III	DSP Classification and Benchmarking	Benchmarking, MIPS, BDTi, EEMBC, More than MIPS: power, code density, Impact of architecture on performance, Comparison of example architectures (ADI, Philips R.E.A.L., TI C55/C6x).
Unit IV	Low power clock distribution	Inter-processor communication, Communication channels, Firmware partitioning problems, Debug and Emulation concepts.
Unit V	Multi-core DSP design	Trend: towards higher performance. Trend: merge microcontrollers with DSPs. Trend: time-to-market: do we need floating point, C hardware.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	J.G.Ackenhausen, Real-Time Signal Processing Design and Implementation of Signal Processing Systems, IEEE Press+Prentice Hall, 2000.
2.	V.K.Madisetti, VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis, IEEE Press+Butterworth-Heinemann, 1998
3.	J. Proakis, D. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Fourth edition, 2006, Prentice-Hall.
4.	K.J.Ray Liu and K.Yao, High Performance VLSI Signal Processing: Systems Design and application, Vol. 2, 1998, IEEE Press.

Course Code	ECVM 572	Semester: (specify Odd/Even)	Session :
Course Name	MOS Devices Modelling and Characterization		
Credits	3	Contact Hours	3
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	• To provide an understanding of operation, modelling and characterization of MOS devices those are inherent to all VLSI circuits.		

Module No.	Title of the Module	List of Topics
Unit I	Basic Concepts	Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.
Unit II	Bias Conditions	CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges. Threshold voltage capacitance voltage relation, The three terminal MOS structure, effect of body bias on surface conditions, Threshold voltage with body bias.
Unit III	MOSFETs	The four terminal Metal Oxide Semiconductor transistor, strong inversion, moderate inversion and weak inversion current, voltage models, Effective mobility, Effect of source and drain series resistance, Temperature effects, Break down.
Unit IV	Small signal models	Ebers-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics
Unit V	Short channel effects	Short channel and thin oxide effects, carrier velocity saturation, channel length modulation, charge sharing, Drain Induced barrier lowering, punch through, Hot carrier effects, Impact ionization, Velocity overshoot, Ballistic operation, Quantum Mechanical effects, DC gate current, Junction leakage, Band to band tunneling, Gate Induced Drain Leakage (GIDL), MOSFET scaling
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2.	Yuan Taur&Tak H Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 2013.
3.	Y. Tsividis& Colin McAndrew, *The MOS Transistor*, 3rd Edition, Oxford University Press, 2013.

4.	Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
5.	E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.

Course Code	**ECVM 573**	**Semester: (specify Odd/Even)**	**Session:**
Course Name	**Mixed Signal IC Design**		
Credits	**3**	**Contact Hours**	3
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	• To understand the necessity of mixed signal IC Designs. • To understand the design and performance measures concept of mixed signal IC circuits.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Basic Concepts	Introduction to analog VLSI and mixed signal issues in CMOS Technologies, MOS transistor: Introduction, Short channel effects, current source and current mirror, Common-Source Amplifier, Source-Follower, Source Degenerated Current Mirrors, cascode Current Mirrors, MOS Differential Pair and Gain Stage, active load, C- MOS circuit.
Unit II	Sampling	Ideal Sampling, Non idealities in sampling, noise and distortion in sampling, sampleand hold circuits, timing issues in sample and hold circuit, bootstrapping systems, charge injection and noise, introduction to switched capacitor circuits, switched capacitor sample and hold circuits, static specifications of data converters, accuracy, nonlinearity, offset, dynamic specifications, SNR, SFDR, ENOB, dynamic range.
Unit III	Data converters	D/A and A/D converters: Introduction A/D and D/A, Various type of A/D converter, ADCs, ramp, tracking, dual slope, successive approximation and flash types, Multi-stage flash type ADCs, Signal-to-Noise Ratio (SNR), Clock Jitter and A Tool: The Spectral Density, Improving SNR using Averaging, Linearity Requirements, Adding a Noise Dither, Jitter, and Anti-Aliasing Filter, Using Feedback to Improve SNR. Passive Noise-Shaping - Signal-to-Noise Ratio and Decimating and Filtering the Modulator's Output, Offset, Matching, and Linearity. Improving SNR and Linearity - Second-Order Passive Noise-Shaping and Passive, Noise-Shaping Using Switched-Capacitors, Increasing SNR using K-Paths and Improving Linearity Using an Active Circuit.
Unit IV	Noise-Shaping Data	First-Order Noise Shaping - Modulation Noise in First-Order NS Modulators, RMS Quantization Noise in a First-Order Modulator, and Decimating and Filtering the Output of a NS

	Converter	Modulator, Pattern Noise from DC Inputs (Limit Cycle Oscillations), Integrator and Forward Modulator Gain, Comparator Gain, Offset, Noise, and Hysteresis, and, Op-Amp Gain (Integrator Leakage) Op-Amp: Settling Time, Offset, Op-Amp Input-Referred Noise, and Practical Implementation of the First-Order NS Modulator, Second–Order Noise Shaping, Second–Order Modulator Topology, Integrator Gain, and Selecting Modulator (Integrator) Gains. Noise–Shaping Topologies – Higher–Order Modulators, Filtering the Output of an M^{th}–Order NS Modulator, Implementing Higher–Order, Single–Stage Modulators, Multi–Bit Modulators, and Error Feedback
Unit V	Band pass and High-Speed Data Converters	Continuous–Time Band pass Noise–Shaping – Passive–Component Band pass Modulators, Active–Component Band pass Modulators, and Modulators for Conversion at Radio Frequencies, Cascaded Modulators, Switched Capacitor Band pass Noise–Shaping – Switched–Capacitor Resonators, Second Order Modulators, Fourth–Order Modulators, and Digital I/Q Extraction to Baseband, Topology of a high–speed data converter – Clock Signals, Implementation, Filtering, Discussion, and Understanding the Clock Signals.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Baker, R. Jacob, "CMOS: mixed-signal circuit design", john Wiley &Sons, 2008.
2.	R. Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, 2nd Edition, Springer, 2007.
3.	R. Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", 2nd Edition, Springer, 2007
4.	M. J. M. Pelgrom, "Analog-to-Digital Conversion", Springer, 2010

Course Code	**ECVM 574**	**Semester: (specify Odd/Even)**	**Session :**
Course Name	**High Speed System (Board level) Design- (includes PCB design, thermal management, power supply)**		
Credits	**3**	**Contact Hours**	3
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	• To address the mechanical aspect of PCB design and to aid in understanding the design issues, manufacturing processes. • To expose the state of art technology in PCB design and manufacturing.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Transmission line theory (basics)	crosstalk and non-ideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise; Practical aspects of measurement at high frequencies; high speed oscilloscopes and logic analyzers

Unit II	Printed Circuit Board	Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation Cooling requirements.
Unit III	IC Assembly	Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging , reliability, wafer level burn – in and test.Single chip packaging: functions, types, materials processes, properties, characteristics, trends.Multi chip packaging: types, design, comparison, trends. Passives: discrete, integrated, embedded –encapsulation and sealing: fundamentals, requirements, materials, processes
Unit IV	Real-Time Characteristics	Interconnect Capacitance, Resistance and Inductance fundamentals; Transmission Lines, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI, Digital and RF Issues. Processing Technologies, Thin Film deposition, Patterning, Metal to Metal joining
Unit V	Reliability	Basic concepts, Environmental interactions. Thermal mismatch and fatigue failures thermo mechanically induced electrically induced chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Tummala, Rao R., "Fundamentals of Microsystems Packaging", McGraw Hill, 2001
2.	Howard Johnson , Martin Graham, "High Speed Digital Design: A Handbook of Black Magic", Prentice Hall, 1993
3.	Stephen H. Hall, Garrett W. Hall, James A. McCal , "High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices",Wiley-IEEE Press, 2000
4.	Tummala, Rao R, "Microelectronics packaging handbook", McGraw Hill, 2008.
5.	Bosshart, "Printed Circuit Boards Design and Technology", Tata McGraw Hill, 1988.