



NATIONAL INSTITUTE OF TECHNOLOGY DELHI
Department of Electronics & Communication Engineering



Organizing
Six Days Short Term Training Programme

HANDS-ON SESSION
on
DIGITAL DESIGN FLOW IN FPGA AND RTL TO GDSII
September 9 to 14, 2024
(Hybrid Mode)

Experts



Prof. R. K. Sharma
NIT Kurukshetra



Prof. Sudeb Dasgupta
IIT Roorkee, India



Prof. Neeta Pandey
DTU Delhi



Prof. Noor Mohd.
IITDM Kancheepuram



Prof. Prathiba A
VIT Chennai



Mr. Upendra Gupta
CoreEL Technologies



Mr. Kumar Divya
CoreEL Technologies



Mr. Anish Kumar
Entuple Technologies

Chief Patron

Prof. (Dr.) Ajay K Sharma
Director, NIT Delhi



Registration

Register for STTP through the following form link
<https://forms.gle/tdRcdVwyDNaGBCdo7>

Last date for registration: September 5, 2024
Participants will be notified via email

Topics to be Covered

- ✓ Modern Digital VLSI Design
- ✓ VLSI architecture for Signal Processing
- ✓ Hands-on: FPGA Architectures and RTL Analysis
- ✓ Hands-on: PYNQ Python Productivity
- ✓ Hands-on: Embedded System Design
- ✓ Hands-on: Custom IP Design
- ✓ Nanometer SRAM Design
- ✓ Hardware Architecture for Encryption Algorithm
- ✓ Hands-on: RTL to GDS II
- ✓ Analog and Digital Design Flow Using Cadence Tool
- ✓ Case Study & Assignment

The registration fee for the course is as follows:

UG/PG/PhD: INR 500
Faculty: INR 800
Industry personals: INR 1000

Deposit the fee in following account or scan to pay:

Account Holder's Name: Director National Institute of
Technology Fee Collection
Account Number: 092901001801
IFSC Code: ICIC0004610
Bank Name & Branch: ICICI Bank, Delhi-NIT Narela Subcity



Scan to Pay

CHIEF PATRON

Prof. (Dr.) Ajay K Sharma
Director, NIT Delhi

PATRON

Dr. Rikmantra Basu
HoD. ECE, NIT Delhi

CONVENOR(s)

Dr. D. Vaithiyathan
Assistant Professor, NIT Delhi

Dr. Preeti Verma
Assistant Professor, NIT Delhi

COORDINATOR(s)

Dr. Baljit Kaur
Assistant Professor, NIT Delhi

Dr. Manish Verma
Assistant Professor, NIT Delhi

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