

NATIONAL INSTITUTE OF TECHNOLOGY DELHI Department of Electronics & Communication Engineering



Organizing
Six Days Short Term Training Programme

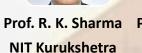
HANDS-ON SESSION

DIGITAL DESIGN FLOW IN FPGA AND RTL TO GDSII

September 9 to 14, 2024 (Hybrid Mode)









na Prof. Sudeb Dasgupta a IIT Roorkee, India



G

Y Prof. Noor Mohd. IITDM Kancheepuram



Prof. Prathiba A VIT Chennai



Mr. Upendra Gupta

CoreEL Technologies

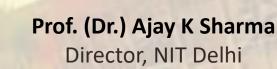




Mr. Kumar Divya CoreEL Technologies

Mr. Anish Kumar Entuple Technologies











Registration

Register for STTP through the following form link https://forms.gle/tdRcdVwyDNaGBCdo7

Last date for registration: September 5, 2024 Participants will be notified via email

Topics to be Covered

- ✓ Modern Digital VLSI Design
- ✓ VLSI architecture for Signal Processing
- ✓ Hands-on: FPGA Architectures and RTL Analysis
- ✓ Hands-on: PYNQ Python Productivity
- ✓ Hands-on: Embedded System Design
- ✓ Hands-on: Custom IP Design
- ✓ Nanometer SRAM Design
- ✓ Hardware Architecture for Encryption Algorithm
- ✓ Hands-on: RTL to GDS II
- ✓ Analog and Digital Design Flow Using Cadence Tool
- ✓ Case Study & Assignment

The registration fee for the course is as follows:

UG/PG/PhD: INR 500 Faculty: INR 800 Industry personals: INR 1000

Deposit the fee in following account or scan to pay:

Account Holder's Name: Director National Institute of **Technology Fee Collection**

Account Number: **IFSC Code:** Bank Name & Branch:

CHIEF PATRON

Prof. (Dr.) Ajay K Sharma Director, NIT Delhi

CONVENOR(s)

CIC0004610

Dr. D. Vaithiyanathan Assistant Professor, NIT Delhi Dr. Preeti Verma

COORDINATOR(s)

Dr. Baljit Kaur Assistant Professor, NIT Delhi

Dr. Manish Verma Assistant Professor, NIT Delhi

Scan to Pay



ICICI Bank, Delhi-NIT Narela Subcity

Dr. Rikmantra Basu HoD. ECE, NIT Delhi

Assistant Professor, NIT Delhi

For any queries Please Contact: Dr. Preeti Verma, Email: preetiverma@nitdelhi.ac.in, Contact No.: +91-9717063730