Scheme and Syllabus
of
M. Tech. ECE (VLSI)
(2024-2025 onwards)

Offered by:

Department of Electronics & Communication Engineering

NATIONAL INSTITUTE OF TECHNOLOGY DELHI

Delhi-110036

(An autonomous Institute under the aegis of Ministry of Education, Govt. of India)

*Approved in the 3rd Meeting of Board of Studies of the Dept. of ECE, held on February 23, 2024 and in line with the recommendation of the Honourable Senate in the 17th Senate Meeting held on May 30, 2024.

Department of Electronics and Communications Engineering
National Institute of Technology Delhi

1.1 About the Department

Welcome to the Department of Electronic and Communication Engineering (ECE), National Institute of Technology Delhi. It was established in 2010, immediately with the beginning of the Institute under the aegis of the Ministry of Human Resource and Development (MHRD), Govt. of India. Currently, Department is offering one Undergraduate Program as B. Tech (ECE) and two Postgraduate programs as M. Tech. ECE and M. Tech. ECE (VLSI). The Department also offers Ph.D. and Post-Doctoral Fellowship (PDF) Programme in relevant areas. It has excellent laboratories and research facilities in electronic devices and circuits, electronic measurement and instrumentation, microprocessor and microcontroller, microwave and antenna design, optical fiber communication and optical device, multimedia, and advanced communication and VLSI design automation and simulation laboratory. The Department has received projects, grants, and fellowships from the Ministry of Electronics and Information Technology (MeitY), the Department of Science and Technology (DST)-SERB, and other funding agencies. The Department has active collaborations with academic & research institutes in India and abroad.

The Department of ECE has a blend of young as well as experienced dynamic faculty members and is committed to providing quality education and research in the field. Faculty members of the department have excellent academic & research credentials and published numerous peer-reviewed journal articles/ papers, Books, Book Chapters, etc. in the diversified field and have adequate experience in advanced research. The department of ECE provides a creative learning environment to the students for excellence in technical education. Here the students learn to face the challenges related to emerging technologies in electronics and communication engineering. The department of ECE promotes a self- learning attitude, entrepreneurial skills, and professional ethics. The department hopes to achieve the national goals and objectives of industrialization and self-reliance. As a result, it hopes to produce post graduates with strong academic and practical backgrounds so that they can fit into the academia, research and industry.

1.2 Vision

Create an educational environment to prepare the students to meet the challenges of the modern electronics and communication industry through state of art technical knowledge and innovative approaches beneficial to society.

1.3 Mission

- To promote teaching and learning by engaging in innovative research and by offering state-of- the-art undergraduate, postgraduate, and doctoral programs.
- To cultivate an entrepreneurial environment and industry interaction leading to the emergence of creators, innovators, and leaders.
- To promote co-curricular and extra-curricular activities for the overall personality development of the students.
- Building of responsible citizens through awareness and acceptance of ethical values

M. Tech. in Electronics and Communication Engineering (VLSI Design)

2.1 Preamble

M. Tech. ECE (VLSI) program offered at NIT Delhi is designed to equip the students with a unique blend of skill sets that include:

- Strong theoretical and experimental foundation
- Predominantly experiment oriented approach with access to well-equipped and specialized laboratories, and supervised internship/ Thesis work.
- Hands-on technical training
- Life skills orientation
- Hard and soft skills
- Business perspective, along with emphasis on innovation and entrepreneurship

2.2 Salient Features:

- Minimum Credits requirements for completion of M. Tech ECE (VLSI) program is 80.
- The Curriculum is based on the guidelines of National Education Policy (NEP) – 2020.
- The curriculum has embedded the Multi Exit/ Multi Entry in the M. Tech program.
- The curriculum is designed to meet the prevailing and ongoing industrial requirements.
- The curriculum includes Project based Education with adequate exposure for Thesis work.
- The curriculum is flexible and offers adequate Choice of Electives (Program Elective Courses).
- The curriculum inherits the Value based Education aims the Holistic Development of the students.
- The Curriculum offers Digital Pedagogy & Flipped Learning with adequate motivation for Entrepreneurship/ Start-ups.

2.3 Cardinal Mention

Students exiting after completing 1st Year will be awarded Post Graduate Diploma in ECE (VLSI) respectively. A minimum Credit requirement for Post Graduate Diploma is 40 Credits

2.4 Program Educational Objectives (PEOs)

PEO-1	To be technically competent in the design, development, and implementation of VLSI circuits and systems to solve complex problems in the domain of electronics and communication.
PEO-2	Students shall be competent in adapting to new technologies for designing and implementation as well as lead research in order to achieve excellence in their professional career.
PEO-3	Enfold the capability to expand horizons beyond engineering for creativity, innovation and entrepreneurship.
PEO-4	Acquire competence and ethics for social and environmental sustainability with a focus on the welfare of humankind.

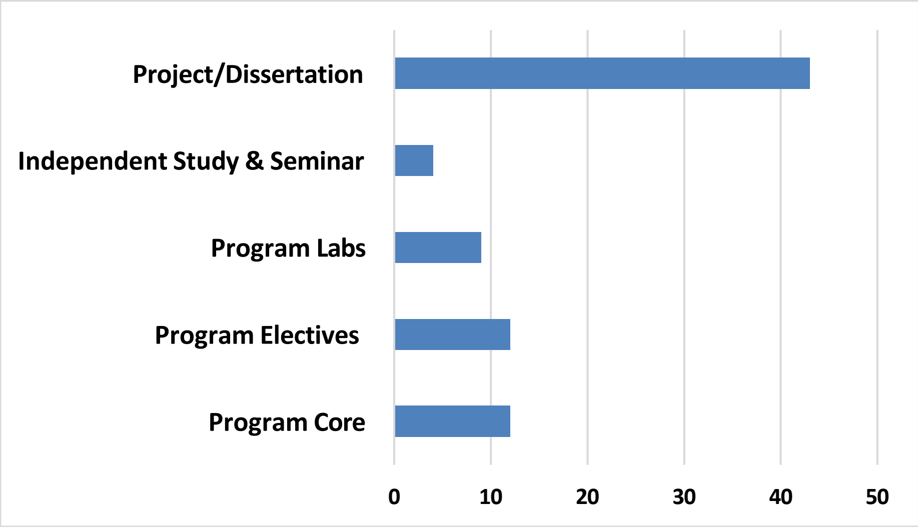
2.5 Program Outcomes (POs)

PO-1	Apply the knowledge of science, mathematics, and engineering principles for a problem-solving attitude and to acquire sound knowledge in the area of the VLSI domain.
PO-2	To design and analyze complex electronic circuits, using appropriate analytical methods as well as front-end and backend tools including prediction and modelling with an understanding of the limitations.
PO-3	An ability to independently carry out research /investigation and development work to solve practical problems and have the preparedness for lifelong learning.
PO-4	Ability to design and conduct experiments, as well as to analyse and interpret data, and synthesis of information.
PO-5	To comprehend and write effective reports and design documentation by adhering to appropriate standards and making effective presentations.
PO-6	Students will have a clear understanding of professional and ethical responsibility.

2.6 Program Specific Objectives (PSOs)

PSO -1	Enable students to get deep knowledge in the domain of VLSI Design and be able to solve complex problems in the field of Electronics and Communication Engineering.
PSO -2	Enable students to carry out research work in emerging technologies and to pursue career in higher studies and research.

3.1 Credit Distribution

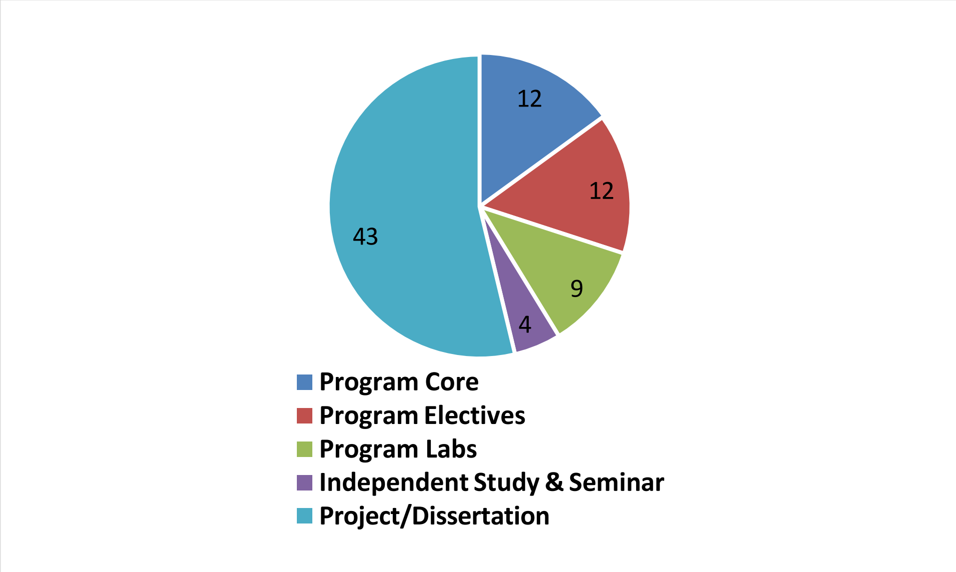


3.2 Semester wise Credit Structure

Credits						
S. No.	Category of Courses	1st Year		2nd Year		Total
		Semester I	Semester II	Semester III	Semester IV	
1.	Program Core	9	3	-	-	**12**
2.	Program Electives	6	6	-	-	**12**
3.	Program Labs	3	6	-	-	**9**
4.	Independent Study & Seminar	2	2	-	-	**4**
5.	Project/Dissertation	-	3	20	20	**43**
Total		**20**	**20**	**20**	**20**	**80**

Minimum Credits Required for Award of Degree = 80

3.3 Credit Distribution (in %)



Course Coding Pattern		
Semester	**M. Tech in ECE**	**M. Tech in ECE (VLSI Design)**
Departmental Core Courses (Theory)		
Autumn Semester	ECEM (5/6)0x (onwards)	ECVM (5/6)0x (onwards)
Spring Semester	ECEM (5/6)5x (onwards)	ECVM (5/6)5x (onwards)
Departmental Elective Courses (Theory)		
Autumn Semester	ECEM (5/6)2x (onwards)	ECVM (5/6)2x (onwards)
Spring Semester	ECEM (5/6)7x (onwards)	ECVM (5/6)7x (onwards)

Numeric for 1st year = 5; Numeric for 2nd year = 6;

Teaching Scheme for
M. Tech in Electronics and Communication Engineering (VLSI Design)

Semester I					
Course Code	**Course Title**	**L**	**T**	**P**	**Credits**
ECVM 5xx	Core - I	3	0	0	3
ECVM 5xx	Core - II	3	0	0	3
ECVM 5xx	Core -III	3	0	0	3
ECVM 5xx	Elective-I	3	0	0	3
ECVM 5xx	Elective-II	3	0	0	3
ECVM 5xx	Lab - I	0	0	6	3
ECVM 507	Independent Study and Seminar	0	0	4	2
Total Credits		**15**	**0**	**10**	**20**

Semester II					
Course Code	**Course Title**	**L**	**T**	**P**	**Credits**
ECVM 5xx	Core IV	3	0	0	3
ECVM 5xx	Elective-III	3	0	0	3
ECVM 5xx	Elective-IV	3	0	0	3
ECVM 5xx	Lab - II	0	0	6	3
ECVM 5xx	Lab - III	0	0	6	3
ECVM 557	Independent Study and Seminar	0	0	4	2
ECVM 558	Minor Project	0	0	6	3
Total Credits		**9**	**0**	**22**	**20**

Semester III					
Course Code	**Course Title**	**L**	**T**	**P**	**Credits**
ECVM 604	Dissertation I	0	0	32	16
ECVM 602	MOOCs Course – I/ Independent Study Course - I	3	0	0	3
ECVM 603	Seminar - I	0	0	2	1
Total Credits		**3**	**0**	**34**	**20**

Semester IV					
Course Code	**Course Title**	**L**	**T**	**P**	**Credits**
ECVM 654	Dissertation II	0	0	32	16
ECVM 652	MOOCs Course – II/ Independent Study Course - II	3	0	0	3
ECVM 653	Seminar - II	0	0	2	1
Total Credits		**3**	**0**	**34**	**20**

Special Note for Selection of Massive Open Online Courses (MOOCs)/ Independent Study Courses
• Students are encouraged to take the above-mentioned MOOCs courses in their 3rd and 4th semesters preferably. The MOOCs courses can only be decided by the students in consultation with the Convener, DPGC (ECE) and HoD (ECE) and should be in allied/ relevant area of VLSI or related to the list of elective courses provided in the scheme. • However, students willing to take those above MOOCs courses during their 1st and 2nd semester are also allowed but their evaluation and marks to be credited during their 3rd and 4th semesters respectively as indicated above. • If a student completes a MOOC course and submits the evaluation result by the end of 3rd and 4th semester respectively, the they will be exempted from appearing for the Institute examination in the respective Independent Study Course – I (in the 3rd semester) and Independent Study Course – II (in the 4th semester). • A student failing to complete the MOOC courses will have to choose an Independent Study course-I (in the 3rd semester) and Independent Study Course – II (in the 4th semester), (*from the list of elective courses and also which is not running in that semester/ previously not studied by the concern student*), have to complete (as per the Institute's procedure) the self-study and examinations as per the Institute's rules and regulations.

List of Core Subjects

S. No.	Course Code	Course Title	L	T	P	Credits	Core Applicability
1.	ECVM 501	Semiconductor Devices	3	0	0	3	Core I + Core II + Core III
2.	ECVM 502	Digital IC Design	3	0	0	3	
3.	ECVM 503	Analog IC Design	3	0	0	3	
4.	ECVM 551	System-on-Programmable Chip Design	3	0	0	3	Core IV

List of Laboratory Subjects

S. No.	Course Code	Course Title	L	T	P	Credits	Lab Applicability
1.	ECVM 505	Analog and Digital Design Laboratory	0	0	6	3	Lab I
2.	ECVM 554	High level Design Laboratory	0	0	6	3	Lab II + Lab III
3.	ECVM 555	System-on-Programmable Chip Design Lab	0	0	6	3	

List of Elective Subjects

S. No.	Course Code	Course Title	L	T	P	Credits	Elective Applicability
1.	ECVM 520	Real Time Signal Processing Systems	3	0	0	3	Elective I + Elective II
2.	ECVM 521	VLSI Systems Design	3	0	0	3	
3.	ECVM 522	Embedded Systems & RTOS	3	0	0	3	
4.	ECVM 523	Architectural Design of IC`s	3	0	0	3	
5.	ECVM 524	VLSI Testing	3	0	0	3	
6.	ECVM 525	RF IC Design	3	0	0	3	
7.	ECVM 526	VLSI Technology	3	0	0	3	
8.	ECVM 527	VLSI Signal Processing	3	0	0	3	
9.	ECVM 528	Block chain Design and Use Cases	3	0	0	3	
10.	ECVM 570	Low Power Design Techniques	3	0	0	3	Elective III + Elective IV
11.	ECVM 571	Mapping Signal Processing Algorithm on DSP Architectures	3	0	0	3	
12.	ECVM 572	MOS Devices Modelling and Characterization	3	0	0	3	
13.	ECVM 573	Mixed Signal IC Design	3	0	0	3	
14.	ECVM 574	High Speed System Design (Board level)	3	0	0	3	
15.	ECVM 575	Advanced Digital System Design	3	0	0	3	

Curriculum in Detail (Core Courses)

Course Code	**ECVM 501**	**Semester: Odd (Specify Odd/Even)**		**Semester: I Session: Autumn**	
Course Name	**Semiconductor Devices**				
Credits	**3**		**Contact Hours**	**3**	
Faculty (Names)	**Coordinator(s)**				
	Teacher(s) (Alphabetically)				
Course Objectives	To make the students understand the fundamentals of electronic devices and to train them to apply these devices in mostly used and important applications.				

Module No.	**Title of the Module**	**List of Topics**
Unit I	Basic Semiconductor Physics	Crystal lattice, energy band model, density of states, distribution statistics – Maxwell- Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, - drift, diffusion, thermionic emission, and tunnelling; excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger, radiative, and surface.
Unit II	Junctions	p-n junctions – fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristic, steady-state and transient conditions, capacitance model, reverse-bias breakdown, SPICE model; metal-semiconductor junctions – fabrication, Schottky barriers, rectifying ad ohmic contacts, I-V characteristics.
Unit III	MOS Capacitors and MOSFETs	The MOS capacitor – fabrication, surface charge –accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; the MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao-Sah and Schichman – Hodges models, I-V characteristic, second-order effects – Velocity saturation, short-channel effects, charge sharing model, hot-carrier effects, gate tunnelling; sub-threshold operation – drain induced barrier lowering (DIBL) effect, unified charge control model (UCCM), SPICE level 1, 2, and 3, and Berkeley short-channel IGFET model (BSIM).

Unit IV	MOSFETs and HEMTs	MESFETs –fabrication, basic operation, Shockley and velocity saturation models, I-V characteristics, high-frequency response, backgating effect, SPICE model; HEMTs – fabrication, modulation (delta) doping, analysis of III-V heterojunctions, charge control, I-V characteristics, SPICE model.
Unit V	BJTs and HBTs	BJTs – fabrication, basic operation, minority carrier distributions and terminal currents, I-V characteristic, switching, second-order effects – base narrowing, avalanche multiplication, high injection, emitter crowding, Kirk effect, etc.; breakdown, high-frequency response, Gummel Poon model, SPICE model; HBTs: - fabrication, basic operation, technological aspects, I-V characteristics, SPICE model.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Ben G. Streetman, Solid State Electronic Devices, Prentice Hall, 1997.
2.	Richard S. Muller and Theodore I. Kamins, Device Electronics for Integrated Circuits, John Wiley, 1986.
3.	S.M. Sze and Kwok K. Ng, Physics of Semiconductor Devices, 3rd edition, John-Wiley, 2006.
4.	Donald Neamen, An Introduction to Semiconductor Devices, McGraw-Hill Education, 2005.

<table>
<tr><td>Course Code</td><td>ECVM 502</td><td colspan="3">Semester: Odd (Specify Odd/Even)</td><td>Semester: I Session: Autumn
Odd</td></tr>
<tr><td>Course Name</td><td colspan="5">DIGITAL IC DESIGN</td></tr>
<tr><td>Credits</td><td colspan="2">3</td><td>Contact Hours</td><td colspan="2">3</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="4"></td></tr>
<tr><td>Teacher(s) (Alphabetically)</td><td colspan="4"></td></tr>
<tr><td>Course Objectives</td><td colspan="5">To introduce the transistor-level design of all digital building blocks and learn all important issues related to size, speed and power consumption.</td></tr>
<tr><td colspan="5">Course Outcomes</td><td>Cognitive Levels</td></tr>
<tr><td>CO1</td><td colspan="4">To be able to use mathematical methods and circuit analysis models in the analysis of CMOS digital circuits.</td><td>Understanding
(Level II)</td></tr>
<tr><td>CO2</td><td colspan="4">To be able to create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort</td><td>Analyzing
(Level IV)</td></tr>
<tr><td>CO3</td><td colspan="4">To be able to design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches</td><td>Evaluating
(Level V)</td></tr>
<tr><td>CO4</td><td colspan="4">To be able to design functional units including ROM and SRAM cell.</td><td>Analyzing
(Level IV)</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="4">List of Topics</td></tr>
<tr><td>I</td><td>MOS Transistor Principles and CMOS Inverter</td><td colspan="4">MOSFET characteristics under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static and Dynamic Characteristics, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.</td></tr>
<tr><td>II</td><td>Combinational logic Circuits</td><td colspan="4">Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.</td></tr>
<tr><td>III</td><td>Sequential Logic Circuits</td><td colspan="4">Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non-Bistable Sequential Circuits.</td></tr>
<tr><td>IV</td><td>Timing Issues in Digital Circuits and Designing Memory</td><td colspan="4">Timing classification of digital systems, Synchronous Design, Self-timed circuit design, Synchronizers and arbiters, Clock synthesis and synchronization using PLL, Distributed clocking using DLLs, Memory core and Peripheral Circuitry.</td></tr>
<tr><td>Course Assessment</td><td colspan="5">Continuous Evaluation 25% Mid Semester 25% End Semester 50%</td></tr>
</table>

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Jan Rabaey, AnanthaChandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2.	N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design", Addision Wesley, 2nd Edition, 1993
3.	K.Martin - Digital integrated circuit design
4.	J.Kuo and J.Lou - Low voltage CMOS VLSI circuits
5.	M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
6.	Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill, 1998.

<table>
<tr><td>Course Code</td><td>ECVM 503</td><td>Semester: Odd (specify Odd/Even)</td><td>Semester: I Session: Autumn</td></tr>
<tr><td>Course Name</td><td colspan="3">ANALOG IC DESIGN</td></tr>
<tr><td>Credits</td><td>3</td><td>Contact Hours</td><td>3</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="2"></td></tr>
<tr><td>Teacher(s) (Alphabetically)</td><td colspan="2"></td></tr>
<tr><td>Course Objectives</td><td colspan="3">To introduce the concepts in analog circuit design relevant to CMOS IC design and to equip students with skills to design and analyze CMOS-based circuits and performance trade-offs.</td></tr>
<tr><td>Course Outcomes:</td><td colspan="3">Understanding the MOS Operation and small signal models.
To analyze single-stage amplifiers with different loads.
To design one, two-stage operational amplifiers and VCO Circuits.
Understanding the role of feedback in amplifiers.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="2">List of Topics</td></tr>
<tr><td>Unit I</td><td>MOS Operation and Models</td><td colspan="2">Basic MOS Device Physics: Device Structure and Operation, General Considerations, MOS I/V Characteristics, Finite Output Resistance in Saturation, Transconductance, Second Order effects: body effect, Channel length modulation, Subthreshold conduction, MOS small signal models, SPICE, Short Channel Effects: DIBL, velocity saturation, hot carrier, impact ionization, surface scattering. (9 hours)</td></tr>
<tr><td>Unit II</td><td>MOS Amplifiers</td><td colspan="2">Amplifiers: Basic concepts, Single Stage Amplifiers: Basic Concepts, Common Source Stage: resistive load, diode connected load, current source load, triode load, source degeneration. Source Follower, Common Gate Stage, Cascode Stage. Folded cascode.
Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. (9 hours)</td></tr>
<tr><td>Unit III</td><td>Frequency Response of Amplifiers</td><td colspan="2">Passive and Active Current Mirrors: Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.
Frequency Response of Amplifiers: Amplifier transfer function, General Considerations, Miller Effect, Common Source Stage, Source Followers, Common Gate Stage. (9 hours)</td></tr>
<tr><td>Unit IV</td><td>Feedback Amplifiers</td><td colspan="2">Feedback Amplifiers: General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers: General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common Mode Feedback, Input Range limitations, VCO Circuit design, phase-locked loop (PLL), delay-locked loop (DLL). (9 hours)</td></tr>
<tr><td>Course Assessment</td><td colspan="3">Continuous Evaluation 25% Mid Semester 25% End Semester 50%</td></tr>
<tr><td colspan="4">Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)</td></tr>
<tr><td>1.</td><td colspan="3">B.Razavi, “Design of Analog CMOS Integrated Circuits”, 2nd Edition, McGraw Hill Edition 2016.</td></tr>
<tr><td>2.</td><td colspan="3">Paul. R.Gray and Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley, 5th Edition, 2009.</td></tr>
<tr><td>3.</td><td colspan="3">R. Jacob Baker, “CMOS Circuit Design, Layout, and Simulation”, 3rd Edition, Wiley, 2010.</td></tr>
<tr><td>4.</td><td colspan="3">T. C. Carusone, D. A. Johns and K. Martin, “Analog Integrated Circuit Design”, 2nd Edition, Wiley, 2012</td></tr>
</table>

Course Code: ECVM 570	**Open course (YES/NO)**	**HM Course (Y/N)**	**DC (Y/N)**		**DE (Y/N)**
	No	**No**	**No**		**Yes**
Type of Course	Theory				
Course Title	**Low Power Design Techniques**				
Course Coordinator					
Course objectives:	The Low Power VLSI Design course focuses on understanding power dissipation sources in digital circuits and applying low-power techniques at the device, circuit, logic, and system levels.				
COURSE OUTCOMES	• Understand the importance of low power in VLSI circuits.				Knowledge (Level I)
	• Understanding of various sources of power dissipation in CMOS circuits.				Understanding (Level II)
	• Analyse the power dissipation at the circuit and gate level.				Analysis (Level IV)
	• Understand and use the concept of power reduction techniques in Clock networks.				Applying (Level III)
Semester	**Autumn:**				
	Lecture	**Tutorial**	**Practical**	**Credits**	**Total Teaching Hours**
Contact Hours	3	0	0	3	36
Prerequisite course code as per proposed course numbers	NIL				
Prerequisite Credits	NIL				
Equivalent course codes as per proposed course and old course	NIL				
Overlap course codes as per proposed course numbers	NIL				
Text Books:					
1.	Title	Practical Low Power Digital VLSI Design			
	Author	Gary K. Yeap			
	Publisher	KAP			
	Edition	2002			
2.	Title	Low Power Design Methodologies			
	Author	Rabaey, Pedram			
	Publisher	Kluwer Academic			

	Edition	
3.	Title	Low-Power CMOS VLSI Circuit Design
	Author	Kaushik Roy, Sharat Prasad
	Publisher	Wiley
	Edition	2000
Content	**Unit I: (09 hours)** Introduction: Need for Low power VLSI Chips, Sources of power dissipation, Dynamic dissipation in CMOS, Short Circuit current in CMOS, CMOS leakage current, Basic principle of Low power design, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. Simulation Power analysis: SPICE circuit simulators, gate-level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, Monte Carlo simulation. **Unit II: (09 hours)** Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. Low Power Circuits: Transistor and gate sizing, Equivalent Pin Ordering, network restructuring, and Reorganization. Special Flip Flops & Latches design, high capacitance nodes, low power digital cells library. **Unit III: (09 hours)** Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components. **Unit IV: (09 hours)** Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs. tolerable skew, Special Techniques: Power Reduction in Clock networks, Clock Gating, CMOS Floating Node, Low Power Bus, Delay balancing, and Low Power Techniques for SRAM.	
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Course Code	**ECVM 551**	**Semester: Odd (Specify Odd/Even)**	**Semester: II Session: Spring Even**
Course Name	**SYSTEM-ON-PROGRAMMABLE CHIP DESIGN**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	To introduce the System-level Design from processor selection to interconnection of all the modules and testing methods.		

Course Outcomes		**Cognitive Levels**
CO1	Ability to apply logical effort techniques for understanding the flow of SoC design.	**Understanding** (Level II)
CO2	Identify & formulate a given problem in the framework of SoC-based design approaches	**Analyzing** (Level IV)
CO3	Design SoC based system for engineering applications	**Evaluating** (Level V)
CO4	Realize the impact of SoC on electronic design philosophy and Macro-electronics thereby inclining towards entrepreneurship & skill development.	**Analyzing** (Level IV)

Module No.	**Title**	**List of Topics**
Unit I	System-level Design	Driving Forces for SoC - Components of SoC - Design flow of SoC - Hardware/Software nature of SoC - Design Trade-offs - SoC Applications, Processor selection - Concepts in Processor Architecture: Instruction set architecture (ISA), Elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom-Designed processors- on-chip memory.
Unit II	Interconnection	On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, CoreConnect, Wishbone, Avalon - Network-on-chip: Architecture-topologies-switching strategies - routing algorithms - flow control, Quality-of-Service-Reconfigurability in communication architectures.
Unit III	IP-based system design	Introduction to IP-based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse – IP integration - IP evaluation on FPGA prototypes.
Unit IV	SOC Implementation and Testing	Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design. Manufacturing test of SoC: Core layer, system layer, application layer- P1500 Wrapper Standardization-SoC Test Automation (STAT).

Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%.
Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Michael J.Flynn, Wayne Luk, "Computer system Design: Systemon-Chip", Wiley-India, 2012
2.	SudeepPasricha, NikilDutt, "On Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
3.	W.H.Wolf, "Computers as Components: Principles of Embedded Computing System Design",Elsevier, 2008.
4.	Patrick Schaumont "A Practical Introduction to Hardware/Software Co-design", 2nd Edition, Springer, 2012.
5.	Wayne Wolf, "Modern VLSI Design: IP Based Design", Prentice-Hall India, Fourth edition, 2009.

Syllabus in Detail (Laboratory Courses)

<table>
<tr><td>Course Code</td><td colspan="2">ECVM 505</td><td colspan="2">Semester: ODD (Specify Odd/Even)</td><td colspan="2">Semester: I Session: Autumn
Month from: July to Dec</td></tr>
<tr><td>Course Name</td><td colspan="6">Design Laboratory (Digital and Analog)</td></tr>
<tr><td>Credits</td><td colspan="3">3</td><td colspan="2">Contact Hours</td><td>6</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td colspan="2">Coordinator(s)</td><td colspan="4"></td></tr>
<tr><td colspan="2">Teacher(s) (Alphabetically)</td><td colspan="4"></td></tr>
<tr><td>Course Objectives</td><td colspan="6">To learn the fundamental principles of VLSI circuit design in digital and analog domain and to provide the exposure in high end hardware tools and technologies.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="5">List of Topics</td></tr>
<tr><td rowspan="3" colspan="2"></td><td colspan="5">I. Digital Experiments (Based on Cadence)
• Study and analysis of the CMOS Inverter circuits.
• Study and analysis of Basing Gates in all type of Static logics.
• Study and analysis of Basing Gates in all type of Dynamic logics.
• Implementation of given Boolean expression in various logics and its analysis.
• Combinational and Sequential logic circuits design implementation.</td></tr>
<tr><td colspan="5">II. Analog / IC Design Experiments (Based on Cadence/Any other equivalent SPICE Circuit Simulator and FPAA based experiments)
• Design and simulation of a simple five transistor differential amplifier – Measure gain, ICMR and CMRR.
• Layout generation, parasitic extraction and re-simulation of the five-transistor differential amplifier.
• Analysis of results of static timing analysis.
• Design, Simulate and implement an inverting gain amplifier, low pass, high pass filters and full wave rectifier. Analyze the frequency response of filters.
• Design and implement a circuit which introduces noise tone to the audio and then bring the original audio by removing the noise tone.</td></tr>
<tr><td colspan="5">Two case studies and one minor project.</td></tr>
<tr><td>Course Assessment</td><td colspan="6">Continuous Evaluation 50% End Semester 50%</td></tr>
</table>

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	SPICE Manual
2.	IRSIM Manual
3.	MAGIC Manual
4.	Xilinx, Vivado Design Suite User Guide.
5.	Cadence Virtuoso Manual

<table>
<tr><td>Course Code</td><td>ECVM 554</td><td colspan="2">Semester: Even
(specify Odd/Even)</td><td colspan="2">Semester: II Session: Spring
Month from: January to May</td></tr>
<tr><td>Course Name</td><td colspan="5">High Level Design Laboratory</td></tr>
<tr><td>Credits</td><td colspan="3">3</td><td>Contact Hours</td><td>6</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="4"></td></tr>
<tr><td>Teacher(s)
(Alphabetically)</td><td colspan="4"></td></tr>
<tr><td>Course Objectives</td><td colspan="5">To learn the Hardware Description Language (Verilog/VHDL) and to provide hands on design experience with hardware/software based embedded system.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="4">List of Topics</td></tr>
<tr><td rowspan="4" colspan="2"></td><td colspan="4">Experiments related to language semantics
- Time Control: delay operator, event control.
- Assignment Types: procedural, blocking, non-blocking, continuous.
- Delay through combinational logic and nets
• Behavioural Coding (examples and problems)
• Structural Coding (examples and problems)
• RT-Level Coding (examples and problems)
• Mixed-Level Coding (examples and problems)
• Coding of state machines and sequential logic
• Coding of test benches
• Coding style for synthesis</td></tr>
<tr><td colspan="4">Entering design constraints and synthesis using "FPGA Express"
- Generating timing reports; CLB/gate usage reports;
Identifying suitable FPGA device (Xilinx) for design implementation.</td></tr>
<tr><td colspan="4">Two case studies</td></tr>
<tr><td colspan="4">Minor project</td></tr>
<tr><td>Course Assessment</td><td colspan="5">Continuous Evaluation 50% End Semester 50%</td></tr>
</table>

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	G. De Micheli, Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994.
2.	P. Kurup and T. Abbasi, Logic Synthesis Using Synopsys, Second Edition, Kluwer, 1996.
3.	J. Bhasker, A VHDL Primer, Third Edition, Prentice-Hall, 1999.
4.	Z. Navabi, Verilog Digital System Design, McGraw-Hill, 1999.
5.	S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice-Hall, 1996.

<table>
<tr><td>Course Code</td><td>ECVM 555</td><td>Semester: Even
(Specify Odd/Even)</td><td colspan="2">Semester: II Session: Spring
Month from: January to May</td></tr>
<tr><td>Course Name</td><td colspan="4">System-on-Programmable Chip Design Lab</td></tr>
<tr><td>Credits</td><td colspan="2">3</td><td>Contact Hours</td><td>6</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="3"></td></tr>
<tr><td>Teacher(s)
(Alphabetically)</td><td colspan="3"></td></tr>
<tr><td>Course Objectives</td><td colspan="4">To Design and develop complete hardware/software systems on an FPGA.</td></tr>
</table>

<table>
<tr><td>Module No.</td><td>Title of the Module</td><td>List of Topics</td></tr>
<tr><td colspan="2" rowspan="3"></td><td>Can be designed around either Xilinx MicroBlaze / Altera NIOS / OpenRISC + Wishbone.
- Implementation of basic SoPC using tools.
- Interfacing with peripherals.
- Creation of custom peripherals using HDL.
- Enhancement of instruction.
- Set with custom instructions.
- Optimizing system architecture through choice of processor enhancements – architecture exploration</td></tr>
<tr><td>Two case studies</td></tr>
<tr><td>Minor project</td></tr>
<tr><td>Course Assessment</td><td colspan="2">Lab: Continuous Evaluation 50% End Semester 50%</td></tr>
</table>

Syllabus in Detail (Elective Courses)

Course Code	**ECVM 520**	**Semester: Odd (Specify Odd/Even)**	**Semester: 1st Session: Autumn**
Course Name	**Real-time Signal Processing Systems**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	To introduce efficient computation method of discrete Fourier transform for the real-time applications, and apply the signal processing algorithms for a wide range of real-time applications.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	The Discrete Fourier Transforms	Discrete Fourier transform, properties of DFT. Frequency domain sampling, Frequency analysis of signals using the DFT. DFT of discrete time signals, Relation between DFT and Z-transform. IDFT.
Unit II	Fast Fourier Transforms	Direct computation of DFT, Need of efficient computation of DFT, Radix-2 Decimation in time domain and decimation in frequency domain algorithms (DIT-FFT and DIF-FFT), Linear filtering methods based on DFT Goertzel Algorithms.
Unit III	Implementation of Discrete time systems	FIR Systems- Direct Form-I, Direct Form-II, Cascade, Parallel structure IIR Systems- Direct Form, Cascade, Linear phase structure, Frequency sampling structure
Unit IV	Design of IIR and FIR filters	Design of digital IIR digital filters from analog filters, Impulse invariance method and bilinear transformation method. Frequency transformations. Design of digital FIR filters using window method.
Unit V	Multirate DSP and Applications	Decimation and Interpolation, Multistage design of interpolators and decimators; Poly-phase decomposition and FIR structures, DSP device architecture and programming (TMS320C6x), Real-time system development, Code Composer Studio and DSP BIOS, Mini project (real-time application of DSP)
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%.	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	S. K. Mitra, “Digital Signal Processing: A Computer-Based Approach”, Third edition, McGraw-Hill, 2006.
2.	J. Proakis, D. Manolakis, “Digital Signal Processing: Principles, Algorithms and Applications”, Fourth edition, Prentice-Hall, 2006
3.	L.R. Rabiner and B. Gold, “Theory and Application of Digital Signal Processing”, First edition, PHI Learning, 2008

<table>
<tr><td>Course Code</td><td colspan="2">ECVM 521</td><td colspan="2">Semester:
(Specify Odd/Even)</td><td colspan="2">Semester: 1st
Session: Autumn</td></tr>
<tr><td>Course Name</td><td colspan="6">VLSI System Design</td></tr>
<tr><td>Credits</td><td colspan="3">3</td><td colspan="2">Contact Hours</td><td>3</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td colspan="2">Coordinator(s)</td><td colspan="4"></td></tr>
<tr><td colspan="2">Teacher(s)
(Alphabetically)</td><td colspan="4"></td></tr>
<tr><td>Course Objectives</td><td colspan="6">To introduce various aspects of VLSI circuits and their design including testing.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="5">List of Topics</td></tr>
<tr><td>Unit I</td><td>Introduction to VLSI Technology</td><td colspan="5">VLSI design methodology, VLSI technology- NMOS, CMOS and BICMOS circuit fabrication. Layout design rules. Stick diagram. Latch up.</td></tr>
<tr><td>Unit II</td><td>MOS Characterization</td><td colspan="5">Characteristics of MOS and CMOS switches. Implementation of logic circuits using MOS and CMOS technology, multiplexers and memory, MOS transistors, threshold voltage, MOS device design equations. MOS models, small-signal AC analysis. CMOS inverters, propagation delay of inverters, Pseudo NMOS, Dynamic CMOS logic circuits, power dissipation.</td></tr>
<tr><td>Unit III</td><td>Logic Synthesis</td><td colspan="5">Programmable logic devices- Antifuse, EPROM and SRAM techniques. Programmable logic cells. Programmable inversion and expander logic. Computation of interconnect delay, Techniques for driving large off-chip capacitors, long lines, Computation of interconnect delays in FPGAs Implementation of PLD, EPROM, EEPROM, static and dynamic RAM in CMOS.</td></tr>
<tr><td>Unit IV</td><td>VLSI Design -Abstraction levels</td><td colspan="5">Different abstraction levels in VLSI design; Design flow as a succession of translations among different abstraction levels; Gajski's Y-Chart; Need for manual designing to move to higher levels of abstraction with automatic translation at lower levels of abstraction; Need to model and validate the design at higher-levels of abstraction and the necessity of HDLs that encompass several levels of design abstraction in their scope.</td></tr>
<tr><td>Unit V</td><td>VLSI Testing</td><td colspan="5">VLSI testing -need for testing, manufacturing test principles, design strategies for test, chip level and system level test techniques.</td></tr>
<tr><td>Course Assessment</td><td colspan="6">Continuous Evaluation 25% Mid Semester 25% End Semester 50%</td></tr>
</table>

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	M. Morris Mano and Michael D. Ciletti, ‘Digital Design’, Pearson, 5th Edition, 2013.
2.	Charles H. Roth, Jr, ‘Fundamentals of Logic Design’, Jaico Books, 4th Edition, 2002.
3.	William I. Fletcher, "An Engineering Approach to Digital Design", Prentice- Hall of India, 1980.
4.	Floyd T.L., "Digital Fundamentals", Charles E. Merril publishing company,1982.
5.	John. F. Wakerly, "Digital Design Principles and Practices", Pearson Education, 4 th Edition,2007.

<table>
<tr><td>Course Code</td><td>ECVM 522</td><td>Semester:
(Specify Odd/Even)</td><td colspan="2">Semester: 1st
Session: Autumn</td></tr>
<tr><td>Course Name</td><td colspan="4">Embedded Systems & RTOS</td></tr>
<tr><td>Credits</td><td colspan="2">3</td><td>Contact Hours</td><td>3</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="3"></td></tr>
<tr><td>Teacher(s)
(Alphabetically)</td><td colspan="3"></td></tr>
<tr><td>Course Objectives</td><td colspan="4">To enable the students to understand and use embedded computing platform.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="3">List of Topics</td></tr>
<tr><td>Unit I</td><td>Embedded Processors</td><td colspan="3">Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.</td></tr>
<tr><td>Unit II</td><td>Embedded Computing Platform</td><td colspan="3">Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock.</td></tr>
<tr><td>Unit III</td><td>Networks</td><td colspan="3">Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.</td></tr>
<tr><td>Unit IV</td><td>Real-Time Characteristic s</td><td colspan="3">Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.</td></tr>
<tr><td>Unit V</td><td>System Design Techniques</td><td colspan="3">Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.</td></tr>
<tr><td>Course Assessment</td><td colspan="4">Theory: Continuous Evaluation 25% Mid Semester 25% End Semester 50%</td></tr>
</table>

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 3rd edition, 2012.
2.	Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia, 2001.
3.	C. M. Krishna and K. G. Shin, “Real-Time Systems” , McGraw-Hill, 1997 .
4.	Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley & Sons, 2002.

<table>
<tr><td>Course Code</td><td>ECVM 523</td><td>Semester:
(Specify Odd/Even)</td><td colspan="2">Semester: 1st
Session: Autumn</td></tr>
<tr><td>Course Name</td><td colspan="4">Architectural Design of IC's</td></tr>
<tr><td>Credits</td><td colspan="2">3</td><td>Contact Hours</td><td>3</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="3"></td></tr>
<tr><td>Teacher(s)
(Alphabetically)</td><td colspan="3"></td></tr>
<tr><td>Course Objectives</td><td colspan="4">This course covers algorithm, architecture and circuit design tradeoffs to optimize for power, performance and area.</td></tr>
</table>

Module No.	Title of the Module	List of Topics
Unit I	Introduction	Introduction: VLSI Design flow, general design methodologies; Mapping algorithms into Architectures: Signal flow graph, data dependences, data path synthesis, control structures, critical path and worst case timing analysis, concept of hierarchical system design.
Unit II	Mapping algorithms into architectures	Data path element: Data path design philosophies, fast adder, multiplier, driver etc., data path optimization, application specific combinatorial and sequential circuit design, CORDIC unit;
Unit III	Pipeline and parallel architectures	Architecture for real time systems, latency and throughput related issues, clocking strategy, power conscious structures, array architectures;
Unit IV	Control strategies	Hardware implementation of various control Structures: micro programmed control techniques, VLIW architecture; Testable architecture: Controllability and Observability, boundary scan and other such techniques, identifying fault locations, self-reconfigurable fault tolerant structures;
Unit V	Issues in timing closure	Static and dynamic timing analysis, System considerations: edge triggered, clock skew, handling asynchronous inputs, sequential machines, clock cycle time, violation-maximum propagation delayrace through, Re-timings
Course Assessment	**Theory**: Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2nd edition, Oxford University Press, New York, 2010.
2.	M. D. Ercegovac and T. Lang, Digital Arithmetic, 1st edition, Elsevier, 2003.
3.	K. Ulrich, Advanced Arithmetic for the Digital Computer, Springer, 2002

Course Code	**ECVM 524**	**Semester: (specify Odd/Even)**	**Semester: 1st** **Session: Autumn**
Course Name	**VLSI Testing**		
Credits	**4**	**Contact Hours**	**3**
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	To study the Design for Testability and the Fault Diagnosis.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Introduction to Testing	Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault, error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits.
Unit II	Fault Models	Fault models, Fault Collapsing, Logic Simulation and Fault simulation, Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms.
Unit III	Combinational circuit test generation	Combinational circuit test generation, Structural Vs Functional test, Path sensitization methods. Difference between combinational and sequential circuit testing, five and eight valued algebras, and Scan chain-based testing method.
Unit IV	Algorithms	D-algorithm procedure, Problems, PODEM Algorithm. Problems on PODEM Algorithm. FAN Algorithm. Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms
Unit V	Built in Self-Test (BIST)	Built in Self-Test (BIST) - Exhaustive pattern generation, random pattern generation, LFSR for pattern generation and Output response analysis, SISR, MISR, Memory BIST – Type of memory faults, fault detection by MARCH tests Issues in test and verification of complex chips, embedded cores and SOCs, System testing and test for SOCs.
Course Assessment	Theory: Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Bushnell Michael and Vishwani Agrawal, *Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*, Vol. 17, Springer Science & Business Media, 2004.
2.	Wang Laung-Terng, Cheng-Wen Wu, and Xiaoqing Wen, *VLSI test principles and architectures: design for testability*, Academic Press, 2006.
3.	AbramoviciMiron, M. A. Breuer and A. D. Friedman, *Digital Systems testing and testable design*, Computer Science Press, 1990.
4.	M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990.
5.	V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989

Course Code	**ECVM 525**	**Semester:** **(Specify Odd/Even)**	**Semester: 1st** **Session: Autumn**
Course Name	**RF IC Design**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	To impart knowledge on basics of CMOS IC design at RF frequencies and to be familiar with the circuits used in RF front end in transceiver design.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Overview of RF Systems	Wireless Transmitter and Receiver Architecture – Heterodyne and SuperHeterodyne Systems - Basic concepts in RF design - units in RF Design, time variance - Effects of Nonlinearity: harmonic distortion, gain compression, cross modulation, intermodulation, cascaded nonlinear stages, AM/PM conversion - Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, representation of noise in circuits
Unit II	High frequency amplifier design	Types of amplifiers: Narrowband and Wideband Amplifiers - zeros as bandwidth enhancers, shunt-series amplifier, f T doublers, neutralization and unilateralization.
Unit III	Need for LNA	Friis' equation - Low noise amplifier design – LNA topologies: noise cancelling LNA topology, distortion cancelling LNA topology - linearity and large signal performance
Unit IV	Need for Mixers	Noise and Linearity trade-off in RF Mixer design-traditional mixer circuits: multiplier-based mixers, subsampling mixers, diode-ring mixers-Noise Folding-Single-sideband and Double-sideband Noise Figure- Feedthrough: Single balanced and Double Balanced – IP3 and IP2 improvement- Oscilators and synthesizers – describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers- phase noise considerations
Unit V	RF power amplifiers	Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations. RFIC simulation and layout-General Layout Issues, Passive and Active
Course Assessment	**Theory**: Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	T.homas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, 2nd ed., Cambridge, UK: Cambridge University Press,2004.
2.	B.Razavi, “RF Microelectronics”, 2nd Ed., Prentice Hall, 1998.
3.	A.A. Abidi, P.R. Gray, and R.G. Meyer, eds., “Integrated Circuits for Wireless Communications”, New York: IEEE Press,1999.
4.	R. Ludwig and P. Bretchko, “RF Circuit Design, Theory and Applications”, Pearson,2000.
5.	Mattuck,A., “Introduction to Analysis”, Prentice-Hall,1998.

<table>
<tr><td>Course Code</td><td colspan="2">ECVM 526</td><td colspan="2">Semester:
(Specify Odd/Even)</td><td>Semester: 1st
Session: Autumn</td></tr>
<tr><td>Course Name</td><td colspan="5">VLSI Technology</td></tr>
<tr><td>Credits</td><td colspan="3">3</td><td>Contact Hours</td><td>3</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td colspan="2">Coordinator(s)</td><td colspan="3"></td></tr>
<tr><td colspan="2">Teacher(s) (Alphabetically)</td><td colspan="3"></td></tr>
<tr><td>Course Objectives</td><td colspan="5">To study the various techniques involved in the VLSI fabrication process.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="4">List of Topics</td></tr>
<tr><td>Unit I</td><td>Introduction to VLSI technology</td><td colspan="4">Device scaling and Moore’s law, basic device fabrication methods, alloy junction and planar process, Czochralski techniques, Characterization methods and wafer specifications, defects in Si and GaAs.</td></tr>
<tr><td>Unit II</td><td>Oxidation, Diffusion and ion-implantation</td><td colspan="4">Types of oxidation and their kinematics, thin oxide growth models, stacking faults, oxidation systems, Deposition process and methods, Diffusion in solids, Diffusion equation and diffusion mechanisms, ion implantation technology, ion implant distributions, implantation damage and annealing, transient enhanced diffusion and rapid thermal processing</td></tr>
<tr><td>Unit III</td><td>Epitaxy and thin film deposition</td><td colspan="4">Thermodynamics of vapor phase growth, MOCVD, MBE, CVD, reaction rate and mass transport limited depositions, APCVD/LPVD, equipments and applications of CVD, PECVD, and PVD.</td></tr>
<tr><td>Unit IV</td><td>Etching</td><td colspan="4">Wet etching, selectivity, isotropy and etch bias, common wet etchants, orientation dependent etching effects; Introduction to plasma technology, plasma etch mechanisms, selectivity and profile control plasma etch chemistries for various films, plasma etch systems.</td></tr>
<tr><td>Unit V</td><td>Lithography</td><td colspan="4">Optical lithography contact/proximity and projection printing, resolution and depth of focus, resist processing methods and resolution enhancement, advanced lithography techniques for nanoscale pattering, immersion, EUV, electron, X-ray lithography.</td></tr>
<tr><td>Course Assessment</td><td colspan="5">Theory: Continuous Evaluation 25% Mid Semester 25% End Semester 50%</td></tr>
<tr><td colspan="6">Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)</td></tr>
</table>

1.	James D. Plummer, “Silicon VLSI Technology: Fundamentals, Practice and Modelling”, Pearson Education, 2000
2.	Sze, S.M., “VLSI Technology”, 4th Ed., Tata McGraw-Hill, 1999
3.	C.Y. Chang and S.M.Sze, “ULSI Technology”, McGraw Hill ,1996
4.	Gandhi, S. K., “VLSI Fabrication Principles: Silicon and Gallium Arsenide”, John Wiley and Sons, 2003.
5.	Stephen A. Campbell, “The Science and Engineering of Microelectronic Fabrication”, 2nd Edition, Oxford University Press 2001

Course Code	**ECVM 527**	**Semester:** **(Specify Odd/Even)**	**Semester: 1st** **Session: Autumn**
Course Name	**VLSI Signal Processing**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	Coordinator(s)		
	Teacher(s) (Alphabetically)		
Course Objectives	To introduce techniques for altering existing DSP structures to suit VLSI implementations.		

Module No.	**Title of the Module**	**List of Topics**
Unit I	Introduction to DSP Systems, Pipelining and Parallel Processing of FIR Filters	Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.
Unit II	Retiming, Algorithmic Strength Reduction	Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.
Unit III	Pipelining and Parallel Processing of IIR Filters	Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.
Unit IV	Bit-Level Arithmetic Architectures	Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.
Unit V	Synchronous, Wave and Asynchronous Pipelining	Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2.	U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2nd Edition, 2004.

<table>
<tr><td>Course Code</td><td>ECVM 528</td><td colspan="2">Semester:
(Specify Odd/Even)</td><td colspan="2">Semester: 1st
Session: Autumn</td></tr>
<tr><td>Course Name</td><td colspan="5">Blockchain Design and Use Cases</td></tr>
<tr><td>Credits</td><td colspan="3">3</td><td>Contact Hours</td><td>3</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="4"></td></tr>
<tr><td>Teacher(s) (Alphabetically)</td><td colspan="4"></td></tr>
<tr><td>Course Objectives</td><td colspan="5">This course provides an overview of Blockchain and its application</td></tr>
</table>

Module No.	**Title of the Module**	**List of Topics**
Unit I	Introduction	Blockchain Components and Concepts, Smart Contracts. Overview of the current financial system and its drawbacks. Advantages of Blockchain as an alternate financial system.
Unit II	Basics of cryptocurrencies	Cryptography, Hash Functions, Public Key Cryptography and Digital Signature.
Unit III	Bitcoin Fundamentals	Bitcoin's block structure, Consensus and mining processes in Bitcoin Bitcoin Trading, Scripting language in Bitcoin.
Unit IV	Permissioned Blockchain	Permissioned Blockchain Architecture, RAFT Consensus, Byzantine General Problem, Practical Byzantine Fault Tolerance.
Unit V	Application of Blockchain	Key Frameworks and Tools, Membership and Identity Management, Hyper ledger composer, Blockchain's implications on Traditional Business, Practical use-cases of Blockchain in Finance, Industry and Governance.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Melanie Swan, "Blockchain: Blueprint for a New Economy", O'Reilly Media, Inc., 2015
2.	Andreas M. Antonopoulos, "Mastering Bitcoin: Unlocking Digital Cryptocurrencies", Second Edition, O'Reilly Media, Inc., 2014

Course Code	**ECVM 571**	**Semester:** **(Specify Odd/Even)**	**Semester: 2nd** **Session: Spring**
Course Name	**Mapping Signal Processing Algorithms on DSP Architectures**		
Credits	**3**	**Contact Hours**	**3**
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	To provide the fundamental bounds on performance, mapping to dedicated and custom resource shared architectures.		
Module No.	**Title of the Module**	**List of Topics**	
Unit I	Introduction to DSP Systems and Algorithms	Digital systems, DSP, computer architecture, DSP computing algorithms, Direct Computing DFT, FFT, Gortzel.	
Unit II	Firmware Development versus Architecture	Digital systems, DSP, computer architecture, DSP development platforms, C compiler, Impact of C on architecture and vice versa, Extensions to C, DSP-C, Simulation Technologies, program verification, Debug and emulation.	
Unit III	DSP Classification and Benchmarking	Benchmarking, MIPS, BDTi, EEMBC, More than MIPS: power, code density, Impact of architecture on performance, Comparison of example architectures (ADI, Philips R.E.A.L., TI C55/C6x).	
Unit IV	Low power clock distribution	Inter-processor communication, Communication channels, Firmware partitioning problems, Debug and Emulation concepts.	
Unit V	Multi-core DSP design	Trend: towards higher performance. Trend: merge microcontrollers with DSPs. Trend: time-to-market: do we need floating point, C hardware.	
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%		

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	J.G.Ackenhausen, Real-Time Signal Processing Design and Implementation of Signal Processing Systems, IEEE Press+Prentice Hall, 2000.
2.	V.K.Madisetti, VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis, IEEE Press+Butterworth-Heinemann, 1998
3.	J. Proakis, D. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Fourth edition, 2006, Prentice-Hall.
4.	K.J.Ray Liu and K.Yao, High Performance VLSI Signal Processing: Systems Design and application, Vol. 2, 1998, IEEE Press.

<table>
<tr><td>Course Code</td><td colspan="2">ECVM 572</td><td colspan="2">Semester:
(Specify Odd/Even)</td><td colspan="2">Semester: 2nd
Session: Spring</td></tr>
<tr><td>Course Name</td><td colspan="6">MOS Devices Modelling and Characterization</td></tr>
<tr><td>Credits</td><td colspan="3">3</td><td colspan="2">Contact Hours</td><td>3</td></tr>
<tr><td rowspan="2">Faculty
(Names)</td><td colspan="2">Coordinator(s)</td><td colspan="4"></td></tr>
<tr><td colspan="2">Teacher(s)
(Alphabetically)</td><td colspan="4"></td></tr>
<tr><td>Course Objectives</td><td colspan="6">To provide an understanding of operation, modelling and characterization of MOS devices those are inherent to all VLSI circuits.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="5">List of Topics</td></tr>
<tr><td>Unit I</td><td>Basic Concepts</td><td colspan="5">Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson’s Equation.</td></tr>
<tr><td>Unit II</td><td>Bias Conditions</td><td colspan="5">CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges. Threshold voltage capacitance voltage relation, The three terminal MOS structure, effect of body bias on surface conditions, Threshold voltage with body bias.</td></tr>
<tr><td>Unit III</td><td>MOSFETs</td><td colspan="5">The four terminal Metal Oxide Semiconductor transistor, strong inversion, moderate inversion and weak inversion current, voltage models, Effective mobility, Effect of source and drain series resistance, Temperature effects, Break down.</td></tr>
<tr><td>Unit IV</td><td>Small signal models</td><td colspan="5">Ebers-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics</td></tr>
<tr><td>Unit V</td><td>Short channel effects</td><td colspan="5">Short channel and thin oxide effects, carrier velocity saturation, channel length modulation, charge sharing, Drain Induced barrier lowering, punch through, Hot carrier effects, Impact ionization, Velocity overshoot, Ballistic operation, Quantum Mechanical effects, DC gate current, Junction leakage, Band to band tunneling, Gate Induced Drain Leakage (GIDL), MOSFET scaling</td></tr>
<tr><td>Course Assessment</td><td colspan="6">Continuous Evaluation 25% Mid Semester 25% End Semester 50%</td></tr>
</table>

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2.	Yuan Taur&Tak H Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 2013.
3.	Y. Tsividis& Colin McAndrew, *The MOS Transistor*, 3rd Edition, Oxford University Press, 2013.
4.	Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
5.	E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.

<table>
<tr><td>Course Code</td><td>ECVM 573</td><td colspan="2">Semester:
(Specify Odd/Even)</td><td>Semester: 2nd
Session: Spring</td></tr>
<tr><td>Course Name</td><td colspan="4">Mixed Signal IC Design</td></tr>
<tr><td>Credits</td><td colspan="2">3</td><td>Contact Hours</td><td>3</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td colspan="2">Coordinator(s)</td><td colspan="2"></td></tr>
<tr><td colspan="2">Teacher(s) (Alphabetically)</td><td colspan="2"></td></tr>
<tr><td>Course Objectives</td><td colspan="4">To understand the design and performance measures concept of mixed signal IC circuits.</td></tr>
<tr><td>Module No.</td><td>Title of the Module</td><td colspan="3">List of Topics</td></tr>
<tr><td>Unit I</td><td>Basic Concepts</td><td colspan="3">Introduction to analog VLSI and mixed signal issues in CMOS Technologies, MOS transistor: Introduction, Short channel effects, current source and current mirror, Common-Source Amplifier, Source-Follower, Source Degenerated Current Mirrors, cascode Current Mirrors, MOS Differential Pair and Gain Stage, active load, C- MOS circuit.</td></tr>
<tr><td>Unit II</td><td>Sampling</td><td colspan="3">Ideal Sampling, Non idealities in sampling, noise and distortion in sampling, sampleand hold circuits, timing issues in sample and hold circuit, bootstrapping systems, charge injection and noise, introduction to switched capacitor circuits, switched capacitor sample and hold circuits, static specifications of data converters, accuracy, nonlinearity, offset, dynamic specifications, SNR, SFDR, ENOB, dynamic range.</td></tr>
<tr><td>Unit III</td><td>Data converters</td><td colspan="3">D/A and A/D converters: Introduction A/D and D/A, Various type of A/D converter, ADCs, ramp, tracking, dual slope, successive approximation and flash types, Multi-stage flash type ADCs, Signal-to-Noise Ratio (SNR), Clock Jitter and A Tool: The Spectral Density, Improving SNR using Averaging, Linearity Requirements, Adding a Noise Dither, Jitter, and Anti-Aliasing Filter, Using Feedback to Improve SNR.
Passive Noise-Shaping - Signal-to-Noise Ratio and Decimating and Filtering the Modulator's Output, Offset, Matching, and Linearity. Improving SNR and Linearity - Second-Order Passive Noise-Shaping and Passive, Noise-Shaping Using Switched-Capacitors, Increasing SNR using K-Paths and Improving Linearity Using an Active Circuit.</td></tr>
<tr><td>Unit IV</td><td>Noise-Shaping Data Converter</td><td colspan="3">First-Order Noise Shaping - Modulation Noise in First-Order NS Modulators, RMS Quantization Noise in a First-Order Modulator, and Decimating and Filtering the Output of a NS Modulator, Pattern Noise from DC Inputs (Limit Cycle Oscillations), Integrator and Forward Modulator Gain, Comparator Gain, Offset, Noise, and Hysteresis, and, Op-Amp Gain (Integrator Leakage)
Op-Amp: Settling Time, Offset, Op-Amp Input-Referred Noise, and Practical Implementation of the First-Order NS Modulator,</td></tr>
</table>

		Second–Order Noise Shaping, Second–Order Modulator Topology, Integrator Gain, and Selecting Modulator (Integrator) Gains. Noise–Shaping Topologies – Higher–Order Modulators, Filtering the Output of an M^{th}–Order NS Modulator, Implementing Higher–Order, Single–Stage Modulators, Multi–Bit Modulators, and Error Feedback
Unit V	Band pass and High-Speed Data Converters	Continuous–Time Band pass Noise–Shaping – Passive–Component Band pass Modulators, Active–Component Band pass Modulators, and Modulators for Conversion at Radio Frequencies, Cascaded Modulators, Switched Capacitor Band pass Noise–Shaping – Switched–Capacitor Resonators, Second Order Modulators, Fourth–Order Modulators, and Digital I/Q Extraction to Baseband, Topology of a high–speed data converter – Clock Signals, Implementation, Filtering, Discussion, and Understanding the Clock Signals.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	Baker, R. Jacob, "CMOS: mixed-signal circuit design", john Wiley &Sons, 2008.
2.	R. Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, 2nd Edition, Springer, 2007.
3.	R. Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", 2nd Edition, Springer, 2007
4.	M. J. M. Pelgrom, "Analog-to-Digital Conversion", Springer, 2010

<table>
<tr><td>Course Code</td><td>ECVM 574</td><td colspan="2">Semester:
(specify Odd/Even)</td><td colspan="2">Semester: 2nd
Session: Spring</td></tr>
<tr><td>Course Name</td><td colspan="5">High Speed System Design (Board level)</td></tr>
<tr><td>Credits</td><td colspan="3">3</td><td>Contact Hours</td><td>3</td></tr>
<tr><td rowspan="2">Faculty (Names)</td><td>Coordinator(s)</td><td colspan="4"></td></tr>
<tr><td>Teacher(s)</td><td colspan="4"></td></tr>
<tr><td>Course Objectives</td><td colspan="5">To expose the state of art technology in PCB design and manufacturing.</td></tr>
</table>

Module No.	**Title of the Module**	**List of Topics**
Unit I	Transmission line theory (basics)	crosstalk and non-ideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high-speed buses; radiated emissions and minimizing system noise; Practical aspects of measurement at high frequencies; high speed oscilloscopes and logic analyzers.
Unit II	Printed Circuit Board	Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation Cooling requirements.
Unit III	IC Assembly	Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging, reliability, wafer level burn – in and test. Single chip packaging: functions, types, materials processes, properties, characteristics, trends. Multi-chip packaging: types, design, comparison, trends. Passives: discrete, integrated, embedded – encapsulation and sealing: fundamentals, requirements, materials, processes.
Unit IV	Real-Time Characteristics	Interconnect Capacitance, Resistance and Inductance fundamentals; Transmission Lines, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI, Digital and RF Issues. Processing Technologies, Thin Film deposition, Patterning, Metal to Metal joining
Unit V	Reliability	Basic concepts, Environmental interactions. Thermal mismatch and fatigue failures thermo mechanically induced electrically induced chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%	

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)	
1.	Tummala, Rao R., “Fundamentals of Microsystems Packaging”, McGraw Hill, 2001
2.	Howard Johnson, Martin Graham, “High Speed Digital Design: A Handbook of Black Magic”, Prentice Hall, 1993
3.	Stephen H. Hall, Garrett W. Hall, James A. McCal , “High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices”, Wiley-IEEE Press, 2000
4.	Tummala, Rao R, “Microelectronics packaging handbook”, McGraw Hill, 2008.
5.	Bosshart, “Printed Circuit Boards Design and Technology”, Tata McGraw Hill, 1988.

Course Code	**ECVM 575**	**Semester:** **(Specify Odd/Even)**	**Session: Spring** **Semester: 2nd**
Course Name	**Advanced Digital System Design**		
Credits	**3**	**Contact Hours**	3
Faculty (Names)	**Coordinator(s)**		
	Teacher(s) (Alphabetically)		
Course Objectives	To provide extended knowledge of digital logic circuits in the form of state model approach and design hazard free circuits. Also, to provide an overview of system design approach using programmable logic devices and gain knowledge about different fault diagnosis and testing methods		
Module No.	**Title of the Module**	**List of Topics**	
Unit I	**Synchronous Sequential Circuit Design:**	Introduction, Moore, Mealy and Mixed Type Synchronous State Machines. Analysis of clocked synchronous sequential circuits and modeling, state diagram, state table, state table assignment and reduction, design of synchronous sequential circuits, design of iterative circuits, ASM chart and realization using ASM.	
Unit II	Asynchronous Sequential Circuit design:	Introduction, Analysis of asynchronous sequential circuit (ASC), Primitive flow table and reduction, type of delays, Cycles and races, state assignment problems and transition table, Excitation Map, Design of ASC, Statics and Dynamic Hazards, Essential hazards. Design vending machine controller, Mixed operating mode asynchronous circuits.	
Unit III	Fault Diagnosis and Testability Algorithms:	Fault table method, Path sensitization method, Boolean difference method, D-Algorithms, Tolerance techniques, The compact algorithms, Practical PLA's, Fault in PLAs, Test Generation, Masking Cycles, DFT Schemes, Built in self test.	
Unit IV	Design using Programmable Logic Devices:	Programming logic device families, Designing of synchronous sequential circuits using PLA/PAL, Realization of finite state machines using PLD, Designing with FPGAs, Xilinx FPGA.	
Course Assessment	Continuous Evaluation 25% Mid Semester 25% End Semester 50%		
Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)			

1.	Donald D.Givone, “Digital Principles and Design”, McGraw Hill, 2nd edition
2.	Shanthi, A. Kavitha, A., Martin Graham, “VLSI Design”, New Age International, 2nd Edition
3.	Uyemura, John P., “CMOS Logic Circuit Design”, Springer 2nd Edition
4.	M.Morris Mano, “Digital Design”, Pearson Education, 3rd edition,.
5.	Charles H.Roth, Jr, “Fundamentals of Logic Design”, Jaico Publishing House, 4th Edition.
5.	Michael D.Ciletti, “Advanced Digital Design with the Verilog HDL”, Pearson Education, 2nd edition