TOPICS TO BE COVERED

- Low Power Reversible Architecture
- Quantum Technology in Semiconductors
- AI for VLSI Design
- Advances in MOS Transistor: From micro to nano
- Recent trends in VLSI Design
- Low Power High Speed Digital Integrated Circuits
- Hands-on Quantum tool
- Hands-on FPGA Flow
- Hands-on Digital Design Flow From RTL to GDS

INVITED SPEAKERS

Chief Guest

Shri Subodh Sachan, Director, STPI HQ

- Mr. Puneet Kumar, Senior Director R/D, Synopsys Inc
- Ms. Shelly Gupta, Founder & Director, AsicGuru Ventures
- Dr. S K Dubey, Sr Principal Scientist, CSIR NPL
- Dr. Trailokya N. Sasamal, NIT Kurukshetra
- Dr. Ratneshwer K Ratnesh, NSUT
- Dr. Shashank Gavel, AI Lead, DataPOEM
- Dr. S R Routray, SRM IST Kattankulathur
- Mr. Anish Kumar, Entuple Tech. Pvt. Ltd.
- Mr. Kumar Divya, CoreEL Tech. Pvt. Ltd.

NATIONAL INSTITUTE OF TECHNOLOGY DELHI

Department of Electronics & Communication Engineering

Organizing

Six Days Short Term Course

On

SILICON TO SYSTEMS:
ADVANCING VLSI DESIGN IN AN AI AND QUANTUM-CONSCIOUS ERA

27 August- 2 September, 2025

(Hybrid Mode)

ENTUPLE TECHNOLOGIES

Chips to Startup Programme

CoreEL Technologies Enabling Excellence

AMD XILINX

इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
सत्यमेव जयते

ABOUT NIT DELHI

An autonomous Institute that functions under the aegis of the Ministry of Education, Govt. of India. It aims to provide instructions and research facilities in various disciplines of Engineering, Science and Technology for advanced learning and dissemination of knowledge. Currently, the institute offers B.Tech. programs in Computer Science and Engg., Electronics and Comm. Engg., Electrical Engg., Civil Engg., Mechanical engg and VLSI Design and Technology. The institute also offers M.Tech., Ph.D., and Post-doctoral programs. NIT Delhi has been ranked 45 by NIRF 2024.

ABOUT THE STC

STC will explore the cutting-edge developments in VLSI design, from nanoscale devices to intelligent system architectures. Focusing on how AI and quantum technologies are shaping the future of chip design and automation. The course bridges theoretical foundations with hands-on exposure to modern design methodologies.

REGISTRATION

Register through the following link

https://forms.gle//B1DJibGoNNe3n6qy8

Last date of registration
20 August, 2025

The registration fee for the course:

UG: INR 400
PG/PhD: INR 600
Faculty: INR 800
Industry personnel: INR 1000
UG (NIT Delhi): INR 300
PG/PhD (NIT Delhi): INR 500

Deposit the fee in following account:
Account Holder's Name: M/S. National Institute of Technology Delhi
Account Number: 092901001915
IFSC Code: ICIC0004610
Bank Name & Branch: ICICI Bank, NIT Delhi

or Scan to Pay

CHIEF PATRON

Prof. (Dr.) Ajay K Sharma
Director, NIT Delhi

PATRON

Dr. Rikmantra Basu
HoD ECE, NIT Delhi

CONVENOR (s)

Dr. Vinay S Pandey
Dr. Preeti Verma

COORDINATOR (s)

Dr. D. Vaithiyanathan
Dr. Manish Verma

For any queries Please Contact: Dr. Preeti Verma **Email:** preetiverma@nitdelhi.ac.in **Contact No.:** +91-9717063730

राष्ट्रीय प्रौद्योगिकी संस्थान दिल्ली
NATIONAL INSTITUTE OF TECHNOLOGY DELHI

TENTATIVE SCHEDULE

STC ON "Silicon to Systems: Advancing VLSI Design in an AI and Quantum-Concious Era"

27 August-2 September 2025, Hybrid Mode (Participant can attend either Online or Physical mode)

	27 Aug. 2025 Wednesday	28 Aug. 2025 Thursday	29 Aug. 2025 Friday	30 Aug. 2025 Saturday	1 September 2025 Monday	2 September 2025 Tuesday
10:00 AM– 12:00 NOON	*Inaugural Session (11.30 AM)*	**Mr. Kumar Divya** **Dr. Manish Verma** **Hands-on** Digital Flow-Digital Circuit/Architecture implementation on FPGA Devices **10:00 AM– 1:00 PM**	**Dr Puneet Kumar** Synopsys Noida **Ms Sheely Gupta** Asic guru Noida	**Dr. Shashank Gavel** Data Poem Bangaluru AI in VLSI	**Mr. Anish** **Dr. D Vaithiynathan** **Dr. Preeti Verma** **Hands-on** Digital Design Flow Using Cadence Tool **10:00 AM– 1:00 PM**	**Dr. Trailokya Nath Sasamal** Low Power Reversible Architecture
Break						
02:00 PM – 04:00 PM	**Dr. Soumya Ranjan Routray** Quantum Technology in Semiconductors	**Mr. Kumar Divya** **Hands-on** Digital Flow-Digital Circuit/Architecture implementation on FPGA Devices **2:00 PM– 5:00 PM**	**Dr. Ratneshwar Kumar Ratnesh** Quantum Computing	**Dr. S K Dubey** CSIR NPL Quantum Devices/Materials	**Mr. Anish** **Dr. D Vaithiynathan** **Dr. Preeti Verma** **Hands-on** Digital Design Flow Using Cadence Tool **2:00 PM– 5:00 PM**	**Dr. Trailokya Nath Sasamal** **Hands-on** Quantum tool