Scheme and Syllabus

of

M. Tech. ECE (VLSI Design)

(2025-2026 onwards)

Offered by:

Department of Electronics & Communication Engineering

NATIONAL INSTITUTE OF TECHNOLOGY DELHI

Delhi-110036

(An autonomous Institute under the aegis of Ministry of Education, Govt. of India)

Department of Electronics and Communications Engineering
National Institute of Technology Delhi

1.1 About the Department

Welcome to the Department of Electronic and Communication Engineering (ECE), National Institute of Technology Delhi. It was established in 2010, immediately with the beginning of the Institute under the aegis of the Ministry of Human Resource and Development (MHRD), Govt. of India. Currently, Department is offering Two Undergraduate Program as B. Tech (ECE) and B.Tech (VLSI Design and Technology) and two Postgraduate programs as M. Tech. ECE and M. Tech. ECE (VLSI). The Department also offers Ph.D. and Post-Doctoral Fellowship (PDF) Programme in relevant areas. It has excellent laboratories and research facilities in electronic devices and circuits, electronic measurement and instrumentation, microprocessor and microcontroller, microwave and antenna design, optical fiber communication and optical device, multimedia, and advanced communication and VLSI design automation and simulation laboratory. The Department has received projects, grants, and fellowships from the Ministry of Electronics and Information Technology (MeitY), the Department of Science and Technology (DST)-SERB, and other funding agencies. The Department has active collaborations with academic & research institutes in India and abroad.

The Department of ECE has a blend of young as well as experienced dynamic faculty members and is committed to providing quality education and research in the field. Faculty members of the department have excellent academic & research credentials and have published numerous peer-reviewed journal articles/ papers, Books, Book Chapters, etc. in diverse fields and have adequate experience in advanced research. The Department of ECE provides a creative learning environment to the students for excellence in technical education. Here, the students learn to face the challenges related to emerging technologies in electronics and communication engineering. The department of ECE promotes a self- learning attitude, entrepreneurial skills, and professional ethics. The department hopes to achieve the national goals and objectives of industrialization and self-reliance. As a result, it hopes to produce post-graduates with strong academic and practical backgrounds so that they can fit into academia, research, and industry.

1.2 Vision

Create an educational environment to prepare the students to meet the challenges of the modern electronics and communication industry through state of art technical knowledge and innovative approaches beneficial to society.

1.3 Mission

- To promote teaching and learning by engaging in innovative research and by offering state-of-the-art undergraduate, postgraduate, and doctoral programs.
- To cultivate an entrepreneurial environment and industry interaction leading to the emergence of creators, innovators, and leaders.
- To promote co-curricular and extra-curricular activities for the overall personality development of the students.
- Building responsible citizens through awareness and acceptance of ethical values

M. Tech. in Electronics and Communication Engineering (VLSI Design)

2.1 Preamble

M. Tech. ECE (VLSI) program offered at NIT Delhi is designed to equip the students with a unique blend of skill sets that include:

- Strong theoretical and experimental foundation
- Predominantly experiment-oriented approach with access to well-equipped and specialized laboratories, and supervised internship/ Thesis work.
- Hands-on technical training
- Life skills orientation
- Hard and soft skills
- Business perspective, along with emphasis on innovation and entrepreneurship

2.2 Salient Features:

- Minimum Credits requirements for completion of M. Tech ECE (VLSI) program is 80.
- The Curriculum is based on the guidelines of National Education Policy (NEP) – 2020.
- The curriculum has embedded the Multi Exit/ Multi Entry in the M. Tech program.
- The curriculum is designed to meet the prevailing and ongoing industrial requirements.
- The curriculum includes Project based Education with adequate exposure for Thesis work.
- The curriculum is flexible and offers adequate Choice of Electives (Program Elective Courses).
- The curriculum inherits the Value based Education aims the Holistic Development of the students.
- The Curriculum offers Digital Pedagogy & Flipped Learning with adequate motivation for Entrepreneurship/ Start-ups.

2.3 Cardinal Mention

Students exiting after completing 1st Year will be awarded Post Graduate Diploma in ECE (VLSI) respectively. A minimum Credit requirement for Post Graduate Diploma is 40 Credits

2.4 Program Educational Objectives (PEOs)

PEO-1	To be technically competent in the design, development, and implementation of VLSI circuits and systems to solve complex problems in the domain of electronics and communication.
PEO-2	Students shall be competent in adapting to new technologies for designing and implementation as well as lead research in order to achieve excellence in their professional career.
PEO-3	Enfold the capability to expand horizons beyond engineering for creativity, innovation and entrepreneurship.
PEO-4	Acquire competence and ethics for social and environmental sustainability with a focus on the welfare of humankind.

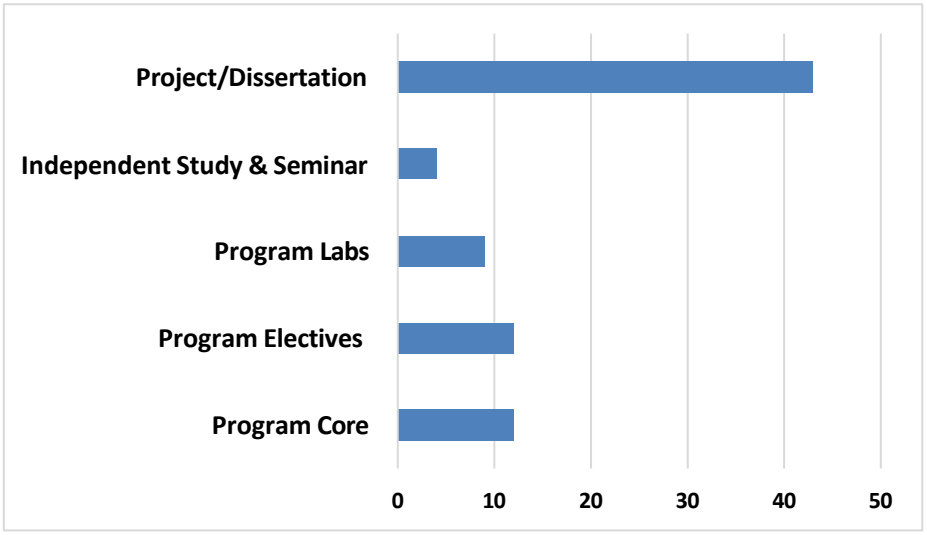
2.5 Program Outcomes (POs)

PO-1	Apply the knowledge of science, mathematics, and engineering principles for a problem-solving attitude and to acquire sound knowledge in the area of the VLSI domain.
PO-2	To design and analyze complex electronic circuits, using appropriate analytical methods as well as front-end and backend tools including prediction and modelling with an understanding of the limitations.
PO-3	An ability to independently carry out research /investigation and development work to solve practical problems and have the preparedness for lifelong learning.
PO-4	Ability to design and conduct experiments, as well as to analyse and interpret data, and synthesis of information.
PO-5	To comprehend and write effective reports and design documentation by adhering to appropriate standards and making effective presentations.
PO-6	Students will have a clear understanding of professional and ethical responsibility.

2.6 Program Specific Objectives (PSOs)

PSO -1	Enable students to get deep knowledge in the domain of VLSI Design and be able to solve complex problems in the field of Electronics and Communication Engineering.
PSO -2	Enable students to carry out research work in emerging technologies and to pursue career in higher studies and research.

3.1 Credit Distribution

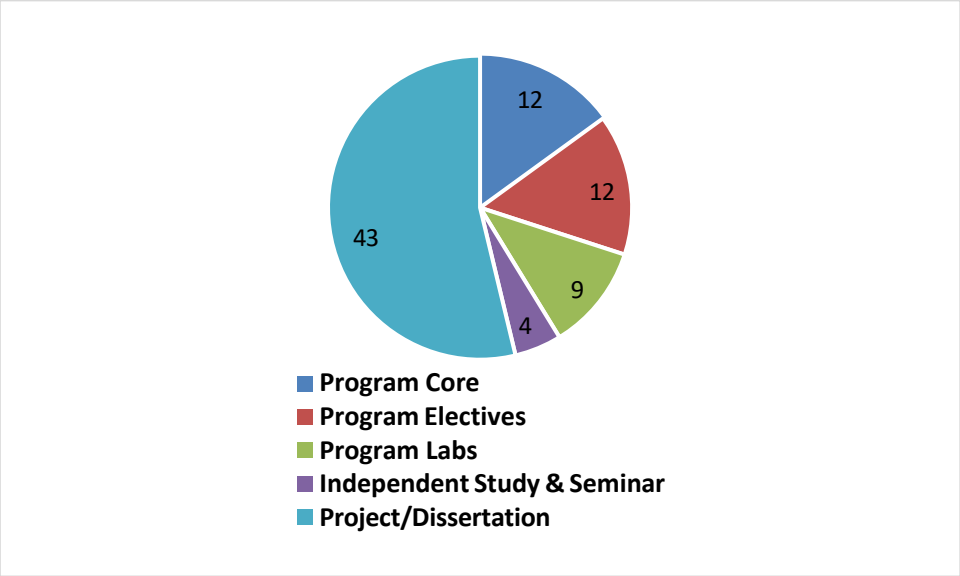


3.2 Semester wise Credit Structure

Credits						
S. No.	**Category of Courses**	**1st Year**		**2nd Year**		**Total**
		Semester I	**Semester II**	**Semester III**	**Semester IV**	
1.	Program Core	9	3	-	-	**12**
2.	Program Electives	6	6	-	-	**12**
3.	Program Labs	3	6	-	-	**9**
4.	Independent Study & Seminar	2	2	-	-	**4**
5.	Project/Dissertation	-	3	20	20	**43**
Total		**20**	**20**	**20**	**20**	**80**

Minimum Credits Required for Award of Degree = 80

3.3 Credit Distribution (in %)



Course Coding Pattern		
Semester	**M. Tech in ECE**	**M. Tech in ECE (VLSI Design)**
Departmental Core Courses (Theory)		
Autumn Semester	ECEM (5/6)0x (onwards)	ECVM (5/6)0x (onwards)
Spring Semester	ECEM (5/6)5x (onwards)	ECVM (5/6)5x (onwards)
Departmental Elective Courses (Theory)		
Autumn Semester	ECEM (5/6)2x (onwards)	ECVM (5/6)2x (onwards)
Spring Semester	ECEM (5/6)7x (onwards)	ECVM (5/6)7x (onwards)

Numeric for 1st year = 5; Numeric for 2nd year = 6;

Teaching Scheme for
M. Tech in Electronics and Communication Engineering (VLSI Design)

Semester I

Course Code	Course Title	L	T	P	Credits
ECVM 5xx	Core - I	3	0	0	3
ECVM 5xx	Core - II	3	0	0	3
ECVM 5xx	Core -III	3	0	0	3
ECVM 5xx	Elective-I	3	0	0	3
ECVM 5xx	Elective-II	3	0	0	3
ECVM 5xx	Lab - I	0	0	6	3
ECVM 507	Independent Study and Seminar	0	0	4	2
Total Credits		**15**	**0**	**10**	**20**

Semester II

Course Code	Course Title	L	T	P	Credits
ECVM 5xx	Core IV	3	0	0	3
ECVM 5xx	Elective-III	3	0	0	3
ECVM 5xx	Elective-IV	3	0	0	3
ECVM 5xx	Lab - II	0	0	6	3
ECVM 5xx	Lab - III	0	0	6	3
ECVM 557	Independent Study and Seminar	0	0	4	2
ECVM 558	Minor Project	0	0	6	3
Total Credits		**9**	**0**	**22**	**20**

Semester III

Course Code	Course Title	L	T	P	Credits
ECVM 604	Dissertation I	0	0	32	16
ECVM 602	MOOCs Course – I/ Independent Study Course - I	3	0	0	3
ECVM 603	Seminar - I	0	0	2	1
Total Credits		**3**	**0**	**34**	**20**

Semester IV

Course Code	Course Title	L	T	P	Credits
ECVM 654	Dissertation II	0	0	32	16
ECVM 652	MOOCs Course – II/ Independent Study Course - II	3	0	0	3
ECVM 653	Seminar - II	0	0	2	1
Total Credits		**3**	**0**	**34**	**20**

Special Note for Selection of Massive Open Online Courses (MOOCs)/ Independent Study Courses

- Students are encouraged to take the above-mentioned MOOC courses in their 3rd and 4th semesters, preferably. The MOOC courses can only be decided by the students in consultation with the Convener, DPGC (ECE), and HoD (ECE) and should be in an allied/ relevant area of VLSI or related to the list of elective courses provided in the scheme.

- However, students willing to take those above MOOCs courses during their 1st and 2nd semesters are also allowed, but their evaluation and marks will be credited during their 3rd and 4th semesters, respectively, as indicated above.

- If a student completes a MOOC course and submits the evaluation result by the end of 3rd and 4th semester, respectively, they will be exempted from appearing for the Institute examination in the respective Independent Study Course – I (in the 3rd semester) and Independent Study Course – II (in the 4th semester).

- A student failing to complete the MOOC courses will have to choose an Independent Study course-I (in the 3rd semester) and Independent Study Course – II (in the 4th semester), (*from the list of elective courses and also which is not running in that semester/ previously not studied by the concern student*), have to complete (as per the Institute's procedure) the self-study and examinations as per the Institute's rules and regulations.

List of Core Subjects

S. No.	Course Code	Course Title	L	T	P	Credits	Core Applicability
1.	ECVM 501	Semiconductor Devices	3	0	0	3	Core I + Core II + Core III
2.	ECVM 502	Digital IC Design	3	0	0	3	
3.	ECVM 503	Analog IC Design	3	0	0	3	
4.	ECVM 551	System-on-Programmable Chip Design	3	0	0	3	Core IV

List of Laboratory Subjects

S. No.	Course Code	Course Title	L	T	P	Credits	Lab Applicability
1.	ECVM 505	Analog and Digital Design Laboratory	0	0	6	3	Lab I
2.	ECVM 554	High-Level Design Laboratory	0	0	6	3	Lab II + Lab III
3.	ECVM 555	System-on-Programmable Chip Design Lab	0	0	6	3	

List of Elective Subjects

S. No.	Course Code	Course Title	L	T	P	Credits	Elective Applicability
1.	ECVM 520	Real-Time Signal Processing Systems	3	0	0	3	Elective I + Elective II
2.	ECVM 521	VLSI Systems Design	3	0	0	3	
3.	ECVM 522	Embedded Systems & RTOS	3	0	0	3	
4.	ECVM 523	Architectural Design of IC`s	3	0	0	3	
5.	ECVM 524	VLSI Testing	3	0	0	3	
6.	ECVM 525	RF IC Design	3	0	0	3	
7.	ECVM 526	VLSI Technology	3	0	0	3	
8.	ECVM 527	VLSI Signal Processing	3	0	0	3	
9.	ECVM 528	Blockchain Design and Use Cases	3	0	0	3	
10.	ECVM 570	Low Power Design Techniques	3	0	0	3	Elective III + Elective IV
11.	ECVM 571	Mapping Signal Processing Algorithm on DSP Architectures	3	0	0	3	
12.	ECVM 572	MOS Devices Modelling and Characterization	3	0	0	3	
13.	ECVM 573	Mixed Signal IC Design	3	0	0	3	
14.	ECVM 574	High Speed System Design (Board level)	3	0	0	3	
15.	ECVM 575	Advanced Digital System Design	3	0	0	3	

Core Courses

Course Title:	**SEMICONDUCTOR DEVICES**
Course Code:	**ECVM 501**
L-T-P:	**3-0-3**
Credits:	**3**
Pre-requisites:	**Engineering Physics / Applied Physics/Electronic Devices and Circuits**

Course Outcomes:		**Cognitive Levels**
CO-1	Define Basic Semiconductor Physics for understanding how electronic devices like diodes and transistor's function.	Remember (Level I)
CO-2	Understand the role of p-n junctions in controlling the flow of current and enabling functionalities like rectification and switching.	Understand (Level II)
CO-3	Apply MOSFET fundamentals of modern integrated circuits, leveraging the metal-oxide-semiconductor structure to control charge flow and enable efficient switching behavior.	Apply (Level III)
CO-4	Evaluate MOSFETs and HEMTs, along with BJTs and HBTs, for analog, digital, and high-frequency circuit applications.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	1	1	1			2	
CO-3	3	1	2	1			2	
CO-4	3	2	2	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:

Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Crystal lattice, energy band model, density of states, distribution statistics– Maxwell- Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, - drift, diffusion, thermionic emission, and tunnelling; excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger, radiative, and surface., characteristics of excess carriers, excess carrier lifetime, introduction to surface effects.	09
Module-II	p-n junctions – fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristic, steady-state and transient conditions, capacitance model, reverse-bias breakdown, SPICE model; metal-semiconductor junctions – fabrication, Schottky barriers, rectifying ad ohmic contacts, I-V characteristics.	09
Module-III	The MOS capacitor – fabrication, surface charge –accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; the MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao-Sah and Schichman – Hodges models, I-V characteristic, second-order effects – Velocity saturation, short-channel effects, charge	09

	sharing model, hot- carrier effects, gate tunnelling; sub-threshold operation – drain induced barrier lowering (DIBL) effect, unified charge control model (UCCM), SPICE level 1, 2, and 3, and Berkeley short-channel IGFET model (BSIM).	
Module-IV	MESFETs –fabrication, basic operation, Shockley and velocity saturation models, I-V characteristics, high-frequency response, backgating effect, SPICE model; HEMTs – fabrication, modulation (delta) doping, analysis of III-V heterojunctions, charge control, I-V characteristics, SPICE model. BJTs – fabrication, basic operation, minority carrier distributions and terminal currents, I-V characteristic, switching, second-order effects – base narrowing, avalanche multiplication, high injection, emitter crowding, Kirk effect, etc.; breakdown, high-frequency response, Gummel Poon model, SPICE model; HBTs: - fabrication, basic operation, technological aspects, I-V characteristics, SPICE model.	09

Textbooks:	1. Ben G. Streetman, Solid State Electronic Devices, Prentice Hall, 1997. 2. S.M. Sze and Kwok K. Ng, Physics of Semiconductor Devices, 3rd edition, John-Wiley, 2006. 3. Donald Neamen, An Introduction to Semiconductor Devices, McGraw-Hill Education, 2005.
Reference Books:	1. Richard S. Muller and Theodore I. Kamins, Device Electronics for Integrated Circuits, John Wiley, 1986.

Course Title:	**DIGITAL IC DESIGN**
Course Code:	**ECVM 502**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Digital Electronics / Digital Logic Design/Analog Electronics**

Course Outcomes:		**Cognitive Levels**
CO-1	Examine the principles of MOS transistors form the foundation for CMOS technology and CMOS inverter.	Remember (Level I)
CO-2	Understand Combinational logic circuits to produce outputs based solely on the current inputs, without any memory or feedback.	Understand (Level II)
CO-3	Apply Sequential logic circuits to determine their outputs based on both current inputs and the history of past inputs, using memory elements like flip-flops.	Apply (Level III)
CO-4	Evaluate Arithmetic building blocks such as adders, multipliers, and ALUs.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:

Module	**Detailed Syllabus**	**Contact Hours**
Module-I	MOSFET characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.	09
Module-II	Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.	09
Module-III	Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non-Bistable Sequential Circuits.	09
Module-IV	Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs Memory Architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers.	09

Text Books:	1. Jan Rabaey, AnanthaChandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003 2. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design", Addision Wesley, 2nd Edition, 1993 3. K.Martin - Digital integrated circuit design 4. J.Kuo and J.Lou - Low voltage CMOS VLSI circuits
Reference Books:	1. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997 2. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill, 1998.

Course Title:	**ANALOG IC DESIGN**
Course Code:	**ECVM 503**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Electronic Devices and Circuits/Analog Electronics**

Course Outcomes:		**Cognitive Levels**
CO-1	Explain the operation, characteristics, and second-order effects of MOS devices, and analyze their small-signal models.	Understand (Level II)
CO-2	Design and analyze MOS-based single-stage and differential amplifiers, including common source, source follower, cascode stages, and Gilbert cells.	Apply (Level III)
CO-3	Evaluate the frequency response of MOS amplifiers and current mirrors, considering the effects of Miller capacitance.	Analyze (Level IV)
CO-4	Study of feedback amplifier systems, operational amplifiers, PLLs, and DLLs.	Apply (Level III)

Course Articulation Matrix:

COs	**PO-1**	**PO-2**	**PO-3**	**PO-4**	**PO-5**	**PO-6**	**PSO-1**	**PSO-2**
CO-1	3	2	-	2	-	-	3	-
CO-2	3	3	2	3	-	-	3	2
CO-3	2	3	2	3	-	-	3	2
CO-4	2	3	3	2	2	2	3	3

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Basic MOS Device Physics: Device Structure and Operation, General Considerations, MOS I/V Characteristics, Finite Output Resistance in Saturation, Transconductance, Second Order effects: body effect, Channel length modulation, Subthreshold conduction, MOS small signal models, SPICE, Short Channel Effects: DIBL, velocity saturation, hot carrier, impact ionization, surface scattering.	09
Module-II	Amplifiers: Basic concepts, Single Stage Amplifiers: Basic Concepts, Common Source Stage: resistive load, diode connected load, current source load, triode load, source degeneration. Source Follower, Common Gate Stage, Cascode Stage. Folded cascode. Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell.	09
Module-III	Passive and Active Current Mirrors: Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Frequency Response of Amplifiers: Amplifier transfer function, General Considerations, Miller Effect, Common Source Stage, Source Followers, Common Gate Stage.	09

Module-IV	Feedback Amplifiers: General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers: General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common Mode Feedback, Input Range limitations, VCO Circuit design, phase-locked loop (PLL), delay-locked loop (DLL).	09

Text Books:	1. B. Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw-Hill Edition 2016. 2. Paul. R.Gray and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009. 3. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010. 4. T. C. Carusone, D. A. Johns and K. Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012 5. P.E.Allen and D.R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
Reference Books:	1. B. Razavi, "Microelectronics", 2nd Edition, Wiely, Reprint 2019.

Course Title:	**SYSTEM-ON-PROGRAMMABLE CHIP DESIGN**
Course Code:	**ECVM 551**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Digital Electronics & Logic Design/ Microprocessors and Microcontrollers**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Gain knowledge of System-level design that involves the integration and optimization of hardware and software components to achieve high-level functionality, performance, and energy efficiency in complex digital systems.	Remember (Level I)
CO-2	Understand Interconnection network of wires and routing structures that link various components on a chip, significantly impacting delay, power consumption, and overall system performance.	Understand (Level II)
CO-3	Apply IP-based system design that leverages reusable Intellectual Property (IP) cores to accelerate the development of complex SoCs, enhancing design productivity and reducing time-to-market.	Apply (Level III)
CO-4	Evaluate SoC implementation and testing in integrating multiple functional blocks on a single chip and validating their functionality using techniques like scan testing and built-in self-test to ensure reliable performance.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Driving Forces for SoC - Components of SoC - Design flow of SoC- Hardware/Software nature of SoC - Design Trade-offs - SoC Applications, Processor Selection-Concepts in Processor Architecture: Instruction set architecture (ISA), Elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom-Designed processors- on-chip memory.	09
Module-II	On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, CoreConnect, Wishbone, Avalon - Network-on-chip: Architecture-topologies-switching strategies - routing algorithms -low control, Quality-of-Service- Reconfigurability in communication architectures.	09
Module-III	Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse – IP integration - IP evaluation on FPGA prototypes.	09

Module-IV	Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design. Manufacturing test of SoC: Core layer, system layer, application layer- P1500 Wrapper Standardization-SoC Test Automation (STAT).	09

Text Books:	1. Michael J. Flynn, Wayne Luk, "Computer system Design: Systemon-Chip", Wiley-India, 2012 2. Sudeep Pasricha, Nikil Dutt, "On Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008. 3. W. H. Wolf, "Computers as Components: Principles of Embedded Computing System Design", Elsevier, 2008.
Reference Books:	1. Patrick Schaumont "A Practical Introduction to Hardware/Software Co-design", 2nd Edition, Springer, 2012. 2. Wayne Wolf, "Modern VLSI Design: IP Based Design", Prentice-Hall India, Fourth edition, 2009.

Laboratory Courses

Course Title:	**DESIGN LABORATORY (DIGITAL AND ANALOG)**
Course Code:	**ECVM 505**
L-T-P:	**0-0-6**
Credits:	**3**
Pre-requisites:	**Digital Electronics & Logic Design**

Course Outcomes:

CO-1	To learn the fundamental principles of VLSI circuit design in digital domain
CO-2	To learn the fundamental principles of VLSI circuit design in analog domain
CO-3	To provide the exposure in high end hardware tools
CO-4	to provide the exposure in high end technologies

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1				2				2
CO-2				2				2
CO-3				2				2
CO-4				2				2

1 - Slightly; 2 - Moderately; 3 - Substantially

List of Experiments:	
1.	I. Digital Experiments (Based on Cadence) • Study and analysis of the CMOS Inverter circuits. • Study and analysis of Basing Gates in all type of Static logics. • Study and analysis of Basing Gates in all type of Dynamic logics. • Implementation of given Boolean expression in various logics and its analysis. Combinational and Sequential logic circuits design implementation.
2.	II. Analog / IC Design Experiments (Based on Cadence/Any other equivalent SPICE Circuit Simulator and FPAA based experiments) • Design and simulation of a simple five transistor differential amplifier – Measure gain, ICMR and CMRR. • Layout generation, parasitic extraction and re-simulation of the five-transistor differential amplifier. • Analysis of results of static timing analysis. • Design, Simulate and implement an inverting gain amplifier, low pass, high pass filters and full wave rectifier. Analyze the frequency response of filters. Design and implement a circuit which introduces noise tone to the audio and then bring the original audio by removing the noise tone.

Learning Resources:

Text Books:	**1.** SPICE Manual **2.** IRSIM Manual **3.** MAGIC Manual **4.** Xilinx, Vivado Design Suite User Guide. **5.** Cadence Virtuoso Manual
Reference Books:	**-**
Other Suggested Readings:	**-**

Course Title:	**HIGH LEVEL DESIGN LABORATORY**
Course Code:	**ECVM 554**
L-T-P:	**0-0-6**
Credits:	**3**
Pre-requisites:	**Digital Electronics & Logic Design**

Course Outcomes:

CO-1	To learn the Hardware Description Language (Verilog/VHDL)
CO-2	To provide hands on design experience with hardware based embedded system
CO-3	To provide hands on design experience with software based embedded system
CO-4	To learn Mix-level design

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1				2				2
CO-2				2				2
CO-3				2				2
CO-4				2				2

1 - Slightly; 2 - Moderately; 3 - Substantially

List of Experiments:	
	Experiments related to language semantics - Time Control: delay operator, event control. - Assignment Types: procedural, blocking, non-blocking, continuous. - Delay through combinational logic and nets • Behavioral Coding (examples and problems) • Structural Coding (examples and problems) • RT-Level Coding (examples and problems) • Mixed-Level Coding (examples and problems) • Coding of state machines and sequential logic • Coding of test benches Coding style for synthesis
	Entering design constraints and synthesis using "FPGA Express" - Generating timing reports; CLB/gate usage reports. Identifying suitable FPGA device (Xilinx) for design implementation.
	Two case studies
	Minor project

Learning Resources:

Text Books:	**1.** G. De Micheli, Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994. **2.** P. Kurup and T. Abbasi, Logic Synthesis Using Synopsys, Second Edition, Kluwer, 1996. **3.** J. Bhasker, A VHDL Primer, Third Edition, Prentice-Hall, 1999.
Reference Books:	1. Z. Navabi, Verilog Digital System Design, McGraw-Hill, 1999. 2. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice-Hall, 1996.

Course Title:	**SYSTEM-ON-PROGRAMMABLE CHIP DESIGN LABORATORY**
Course Code:	**ECVM 555**
L-T-P:	**0-0-6**
Credits:	**3**
Pre-requisites:	**Digital Electronics & Logic Design**

Course Outcomes:

CO-1	To provide students with hands-on experience in designing, developing.
CO-2	To provide testing complex systems built on programmable hardware platforms, often involving both hardware and software components
CO-3	To equip students with the skills to analyze system requirements, perform hardware/software tradeoffs, and implement custom hardware accelerators
CO-4	To improve understanding the intricacies of system-level design, including on-chip buses and interface design

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1				2				2
CO-2				2				2
CO-3				2				2
CO-4				2				2

1 - Slightly; 2 - Moderately; 3 - Substantially

List of Experiments:	
	Can be designed around either Xilinx MicroBlaze / Altera NIOS / OpenRISC + Wishbone. - Implementation of basic SoPC using tools. - Interfacing with peripherals. - Creation of custom peripherals using HDL. - Enhancement of instruction. - Set with custom instructions. Optimizing system architecture through choice of processor enhancements – architecture exploration
	Entering design constraints and synthesis using "FPGA Express" - Generating timing reports; CLB/gate usage reports. Identifying suitable FPGA device (Xilinx) for design implementation.
	Two case studies
	Minor project

Elective Courses

Course Title:	**REAL-TIME SIGNAL PROCESSING SYSTEMS**
Course Code:	**ECVM 520**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Signals and Systems/Digital Signal Processing**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Examine Discrete Fourier Transform (DFT) to convert a finite sequence of equally spaced time-domain samples into a sequence of frequency-domain components.	Remember (Level I)
CO-2	Understand the Fast Fourier Transform (FFT) as an efficient algorithm used to compute the Discrete Fourier Transform (DFT) and its inverse, significantly reducing computational complexity.	Understand (Level II)
CO-3	Apply discrete-time systems in realizing digital filters and signal processing algorithms using structures such as direct form, cascade, or parallel configurations.	Apply (Level III)
CO-4	Evaluate the design of IIR and FIR filters, along with multirate digital signal processing (DSP) in applications such as data compression, efficient signal transmission and adaptive filtering.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:

Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Discrete Fourier transform, properties of DFT. Frequency domain sampling, Frequency analysis of signals using the DFT. DFT of discrete time signals, Relation between DFT and Z-transform. IDFT.	09
Module-II	Direct computation of DFT, Need of efficient computation of DFT, Radix-2 Decimation in time domain and decimation in frequency domain algorithms (DIT-FFT and DIF-FFT), Linear filtering methods based on DFT Goertzel Algorithms.	09
Module-III	FIR Systems- Direct Form-I, Direct Form-II, Cascade, Parallel structure IIR Systems- Direct Form, Cascade, Linear phase structure, Frequency sampling structure	09
Module-IV	Design of digital IIR digital filters from analog filters, Impulse invariance method and bilinear transformation method. Frequency transformations. Design of digital FIR filters using window method. Decimation and Interpolation, Multistage design of interpolators and decimators; Poly-phase decomposition and FIR structures, DSP device architecture and programming (TMS320C6x), Real-time system development, Code Composer Studio and DSP BIOS, Mini project (real-time application of DSP)	09

Text Books:	1. S. K. Mitra, "Digital Signal Processing: A Computer-Based Approach", Third edition, McGraw-Hill, 2006. 2. J. Proakis, D. Manolakis, "Digital Signal Processing: Principles, Algorithms and Applications", Fourth edition, Prentice-Hall, 2006 3. L.R. Rabiner and B. Gold, "Theory and Application of Digital Signal Processing", First edition, PHI Learning, 2008
Reference Books:	1. Kuo, S.M., 2003. Real-time digital signal processing: implementations, applications, and experiments with the TMS320C55X.

Course Title:	**VLSI SYSTEM DESIGN**
Course Code:	**ECVM 521**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Electronic Devices and Circuits/ IC Fabrication Technology**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Introduction to VLSI Technology involves understanding the processes, techniques, and materials used to fabricate integrated circuits at a very large scale, enabling the design of compact, high-performance electronic systems.	Remember (Level I)
CO-2	Understand MOS Characterization, analyzing and evaluating the electrical properties of MOS (Metal-Oxide-Semiconductor) devices, such as threshold voltage, mobility, subthreshold slope, and capacitance.	Understand (Level II)
CO-3	Apply Logic synthesis process of converting a high-level hardware description (such as in Verilog or VHDL) into an optimized gate-level representation.	Apply (Level III)
CO-4	Evaluate VLSI Design abstraction levels—such as behavioral, RTL, gate, and layout levels—to manage complexity, and VLSI Testing.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	VLSI design methodology, VLSI technology- NMOS, CMOS and BICMOS circuit fabrication. Layout design rules. Stick diagram. Latch up.	09
Module-II	Characteristics of MOS and CMOS switches. Implementation of logic circuits using MOS and CMOS technology, multiplexers and memory, MOS transistors, threshold voltage, MOS device design equations. MOS models, small-signal AC analysis. CMOS inverters, propagation delay of inverters, Pseudo NMOS, Dynamic CMOS logic circuits, power dissipation.	09
Module-III	Programmable logic devices- Antifuse, EPROM and SRAM techniques. Programmable logic cells. Programmable inversion and expander logic. Computation of interconnect delay, Techniques for driving large off-chip capacitors, long lines, Computation of interconnect delays in FPGAs Implementation of PLD, EPROM, EEPROM, static and dynamic RAM in CMOS.	09

Module-IV	Different abstraction levels in VLSI design; Design flow as a succession of translations among different abstraction levels; Gajski's Y-Chart; Need for manual designing to move to higher levels of abstraction with automatic translation at lower levels of abstraction; Need to model and validate the design at higher-levels of abstraction and the necessity of HDLs that encompass several levels of design abstraction in their scope. VLSI testing -need for testing, manufacturing test principles, design strategies for test, chip level and system level test techniques	09

Text Books:	1. M. Morris Mano and Michael D. Ciletti, 'Digital Design', Pearson, 5th Edition, 2013. 2. Charles H. Roth, Jr, 'Fundamentals of Logic Design', Jaico Books, 4th Edition, 2002. 3. William I. Fletcher, "An Engineering Approach to Digital Design", Prentice- Hall of India, 1980. 4. Floyd T.L., "Digital Fundamentals", Charles E. Merril publishing company,1982. 5. John. F. Wakerly, "Digital Design Principles and Practices", Pearson Education, 4 th Edition,2007.
Reference Books:	1. B.Razavi, "RF Microelectronics", 2nd Ed., Prentice Hall, 1998.

Course Title:	**EMBEDDED SYSTEMS & RTOS**
Course Code:	**ECVM 522**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Computer Organization and Architecture/Microprocessors and Microcontrollers**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Introduction to Embedded processors for specific applications like automotive control, medical devices, and consumer electronics.	Remember (Level I)
CO-2	Understand Embedded Computing Platform as a specialized system combining hardware and software to perform dedicated tasks efficiently.	Understand (Level II)
CO-3	Apply Networks to enable communication and data exchange between interconnected devices or systems.	Apply (Level III)
CO-4	Evaluate Real-time characteristics and system design techniques focus on ensuring timely and predictable responses in embedded systems.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioral Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.	09
Module-II	Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example: Alarm Clock.	09
Module-III	Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, System performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator	09

	Controller.	
Module-IV	Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling. Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.	09

Text Books:	1. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers, 3rd edition, 2012. 2. Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia, 2001. 3. C. M. Krishna and K. G. Shin, "Real-Time Systems", McGraw-Hill, 1997. 4. Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley & Sons, 2002.
Reference Books:	1. Wang, J., 2017. Real-time embedded systems. John Wiley & Sons.

Course Title:	**ARCHITECTURAL DESIGN OF IC'S**
Course Code:	**ECVM 523**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**VLSI Design / CMOS Design/Algorithms and Data Structures**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Introduction to Architectural design of ICs defining the high-level structure and functional organization of integrated circuits to optimize performance, area, and power.	Remember (Level I)
CO-2	Understand Mapping algorithms to the process of translating computational algorithms into efficient hardware implementations by aligning algorithmic operations with architectural resources such as processing units, memory, and interconnects.	Understand (Level II)
CO-3	Apply Pipeline and parallel architectures hardware design strategies that enhance computational speed and efficiency by overlapping instruction execution and distributing tasks across multiple processing units.	Apply (Level III)
CO-4	Evaluate Control strategies and timing in digital design to ensure correct data sequencing and synchronization, addressing challenges in meeting timing constraints across complex circuits.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Introduction: VLSI Design flow, general design methodologies; Mapping algorithms into Architectures: Signal flow graph, data dependences, data path synthesis, control structures, critical path and worst-case timing analysis, concept of hierarchical system design.	09
Module-II	Data path element: Data path design philosophies, fast adder, multiplier, driver etc., data path optimization, application specific combinatorial and sequential circuit design, CORDIC unit;	09
Module-III	Architecture for real time systems, latency and throughput related issues, clocking strategy, power conscious structures, array architectures;	09
Module-IV	Hardware implementation of various control Structures: micro programmed control techniques, VLIW architecture; Testable architecture: Controllability and Observability, boundary scan and other such techniques, identifying fault locations, self-	09

	reconfigurable fault tolerant structures. Static and dynamic timing analysis, System considerations: edge triggered, clock skew, handling asynchronous inputs, sequential machines, clock cycle time, violation-maximum propagation delay race through, Re-timings	

Text Books:	1. B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2nd edition, Oxford University Press, New York, 2010. 2. M. D. Ercegovac and T. Lang, Digital Arithmetic, 1st edition, Elsevier, 2003. 3. K. Ulrich, Advanced Arithmetic for the Digital Computer, Springer, 2002
Reference Books:	1. Razavi, B., 2020. Design of CMOS phase-locked loops: from circuit level to architecture level. Cambridge University Press.

Course Title:	**VLSI TESTING**
Course Code:	**ECVM 524**
L-T-P:	**3-0-0**
Credits:	**4**
Pre-requisites:	**VLSI Design / CMOS Design/Digital Electronics / Digital Logic Design**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Introduction to testing involves verifying and validating integrated circuits to ensure correct functionality, reliability, and performance under various operating conditions.	Remember (Level I)
CO-2	Understand Fault models of possible defects in digital circuits used to design and evaluate test strategies for detecting and diagnosing errors.	Understand (Level II)
CO-3	Apply Combinational circuit test generation creating input patterns to detect faults in logic circuits without memory elements, ensuring correctness of outputs for all logic conditions.	Apply (Level III)
CO-4	Evaluate Algorithms for Built-In Self-Test (BIST) to enable integrated circuits to test themselves using embedded hardware and software mechanisms, improving fault coverage and reducing reliance on external test equipment.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault, error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits.	09
Module-II	Fault models, Fault Collapsing, Logic Simulation and Fault simulation, Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms.	09
Module-III	Combinational circuit test generation, Structural Vs Functional test, Path sensitization methods. Difference between combinational and sequential circuit testing, five and eight valued algebras, and Scan chain-based testing method.	09

Module-IV	D-algorithm procedure, Problems, PODEM Algorithm. Problems on PODEM Algorithm. FAN Algorithm. Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithm Built in Self-Test (BIST) - Exhaustive pattern generation, random pattern generation, LFSR for pattern generation and Output response analysis, SISR, MISR, Memory BIST – Type of memory faults, fault detection by MARCH tests Issues in test and verification of complex chips, embedded cores and SOCs, System testing and test for SOCs.	09

Text Books:	1. Bushnell Michael and Vishwani Agrawal, *Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*, Vol. 17, Springer Science & Business Media, 2004. 2. Wang Laung-Terng, Cheng-Wen Wu, and Xiaoqing Wen, *VLSI test principles and architectures: design for testability*, Academic Press, 2006. 3. AbramoviciMiron, M. A. Breuer and A. D. Friedman, *Digital Systems testing and testable design*, Computer Science Press, 1990.
Reference Books:	1. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990. 2. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989

Course Title:	**RF IC DESIGN**
Course Code:	**ECVM 525**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Analog Electronics / Electronic Circuits**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	An overview of RF systems includes the fundamental principles, components, and design considerations involved in transmitting and receiving radio frequency signals for communication applications.	Remember (Level I)
CO-2	Understand High-frequency amplifier design on developing amplifiers that operate efficiently at RF or microwave frequencies, emphasizing gain, bandwidth, impedance matching, stability, and noise performance.	Understand (Level II)
CO-3	Apply Low Noise Amplifier (LNA) in enhancing the sensitivity of a receiver system by amplifying very weak signals while adding minimal noise and preserving signal integrity in RF and communication applications.	Apply (Level III)
CO-4	Evaluate Mixers shift signal frequencies, while RF power amplifiers boost signal strength for transmission.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Wireless Transmitter and Receiver Architecture – Heterodyne and Superheterodyne Systems - Basic concepts in RF design - units in RF Design, time variance - Effects of Nonlinearity: harmonic distortion, gain compression, cross modulation, intermodulation, cascaded nonlinear stages, AM/PM conversion - Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, representation of noise in circuits	09
Module-II	Types of amplifiers: Narrowband and Wideband Amplifiers - zeros as bandwidth enhancers, shunt-series amplifier, f T doublers, neutralization and unilateralization.	09
Module-III	Friis' equation - Low noise amplifier design – LNA topologies: noise cancelling LNA topology, distortion cancelling LNA topology - linearity and large signal performance	09
Module-IV	Friis' equation - Low noise amplifier design – LNA topologies: noise cancelling LNA topology, distortion cancelling LNA	09

	topology - linearity and large signal performance Noise and Linearity trade-off in RF Mixer design-traditional mixer circuits: multiplier-based mixers, subsampling mixers, diode-ring mixers-Noise Folding-Single-sideband and Double-sideband Noise Figure-Feedthrough: Single balanced and Double Balanced – IP3 and IP2 improvement- Oscillators and synthesizers – describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers- phase noise considerations Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations. RFIC simulation and layout-General Layout Issues, Passive and Active	

Text Books:	1. T.homas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", 2nd ed., Cambridge, UK: Cambridge University Press,2004. 2. B.Razavi, "RF Microelectronics", 2nd Ed., Prentice Hall, 1998. 3. A.A. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press,1999.
Reference Books:	1. R. Ludwig and P. Bretchko, "RF Circuit Design, Theory and Applications", Pearson,2000. 2. Mattuck, A., "Introduction to Analysis", Prentice-Hall,1998.

Course Title:	**VLSI TECHNOLOGY**
Course Code:	**ECVM 526**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Electronic Devices and Circuits/Solid-State Devices / Semiconductor Physics**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Gain foundational knowledge of VLSI technology.	Remember (Level I)
CO-2	Understand the principles of diffusion and oxidation.	Understand (Level II)
CO-3	To Study epitaxy and etching mechanisms.	Apply (Level III)
CO-4	Understand the principles of lithography in VLSI fabrication	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Device scaling and Moore's law, basic device fabrication methods, alloy junction and planar process, Czochralski techniques, Characterization methods and wafer specifications, defects in Si and GaAs.	09
Module-II	Types of oxidations and their kinematics, thin oxide growth models, stacking faults, oxidation systems, Deposition process and methods, Diffusion in solids, Diffusion equation and diffusion mechanisms, ion implantation technology, ion implant distributions, implantation damage and annealing, transient enhanced diffusion and rapid thermal processing	09
Module-III	Thermodynamics of vapor phase growth, MOCVD, MBE, CVD, reaction rate and mass transport limited depositions, APCVD/LPVD, equipment and applications of CVD, PECVD, and PVD. Wet etching, selectivity, isotropy and etch bias, common wet etchants, orientation dependent etching effects; Introduction to plasma technology, plasma etch mechanisms, selectivity and profile control plasma etch chemistries for various films, plasma etch systems.	09
Module-IV	Optical lithography contact/proximity and projection printing, resolution and depth of focus, resist processing methods and resolution enhancement, advanced lithography techniques for nanoscale pattering, immersion, EUV, electron, X-ray lithography.	09

Learning Resources:

Text Books:	1. James D. Plummer, "Silicon VLSI Technology: Fundamentals, Practice and Modelling", Pearson Education, 2000 2. Sze, S.M., "VLSI Technology", 4th Ed., Tata McGraw Hill, 1999 3. C.Y. Chang and S.M.Sze, "ULSI Technology", McGraw Hill ,1996
Reference Books:	1. Gandhi, S. K., "VLSI Fabrication Principles: Silicon and Gallium Arsenide", John Wiley and Sons, 2003. 2. Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", 2nd Edition, Oxford University Press 2001

Course Title:	**VLSI SIGNAL PROCESSING**
Course Code:	**ECVM 527**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Digital Signal Processing (DSP)**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Analyze data flow graphs to determine critical path, loop bound, and iteration bound for performance optimization in DSP systems.	Remember (Level I)
CO-2	Examine retiming and unfolding techniques to reduce sample period and enhance parallel processing efficiency in DSP architectures	Understand (Level II)
CO-3	Apply pipelined and parallel recursive filters using look-ahead pipelining and fast convolution algorithms.	Apply (Level III)
CO-4	Evaluate bit-level arithmetic architectures and strength reduction techniques for low-power and high-speed DSP implementation.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.	09
Module-II	Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.	09
Module-III	Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power- of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.	09
Module-IV	Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-	09

	serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters. Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.	

Learning Resources:

Text Books:	1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007. 2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2nd Edition, 2004.
Reference Books:	1. Parhi, K.K., 2007. VLSI digital signal processing systems: design and implementation. John Wiley & Sons.

Course Title:	**BLOCKCHAIN DESIGN AND USE CASES**
Course Code:	**ECVM 528**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Introduction to Programming**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Explain the components of blockchain technology and analyze its advantages over traditional financial systems.	Remember (Level I)
CO-2	Analyze cryptographic principles including hash functions, public key cryptography, and digital signatures essential for blockchain security.	Understand (Level II)
CO-3	Apply the structure, consensus mechanisms, and scripting functionality of the Bitcoin blockchain.	Apply (Level III)
CO-4	Evaluate permissioned blockchain concepts, consensus algorithms, and identity frameworks to real-world use cases in business and governance.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:

Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Blockchain Components and Concepts, Smart Contracts. Overview of the current financial system and its drawbacks. Advantages of Blockchain as an alternate financial system.	09
Module-II	Cryptography, Hash Functions, Public Key Cryptography and Digital Signature.	09
Module-III	Bitcoin's block structure, Consensus and mining processes in Bitcoin Bitcoin Trading, Scripting language in Bitcoin.	09
Module-IV	Permissioned Blockchain Architecture, RAFT Consensus, Byzantine General Problem, Practical Byzantine Fault Tolerance. Key Frameworks and Tools, Membership and Identity Management, Hyper ledger composer, Blockchain's implications on Traditional Business, Practical use-cases of Blockchain in Finance, Industry and Governance.	09

Learning Resources:

Text Books:	1. Melanie Swan, "Blockchain: Blueprint for a New Economy", O'Reilly Media, Inc., 2015 2. Andreas M. Antonopoulos, "Mastering Bitcoin: Unlocking Digital Cryptocurrencies", Second Edition, O'Reilly Media, Inc., 2014
Reference Books:	1. Julie, E.G., Nayahi, J.J.V. and Jhanjhi, N.Z. eds., 2020. Blockchain Technology: Fundamentals, Applications, and Case Studies. CRC Press.

Course Title:	**LOW POWER DESIGN TECHNIQUES**
Course Code:	**ECVM 570**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**VLSI Design / CMOS Digital Integrated Circuits**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Describe the need for low-power VLSI design and identify different sources of power dissipation in CMOS circuits.	Understand (Level II)
CO-2	Explain simulation and probabilistic power analysis techniques for estimating power in VLSI systems.	Understand (Level II)
CO-3	Apply basic low-power design techniques such as transistor sizing, logic restructuring, and signal gating to reduce power consumption.	Apply (Level III)
CO-4	Discuss power reduction strategies in clock distribution and memory systems for low-power VLSI design.	Understand (Level II)

Course Articulation Matrix:

COs	**PO-1**	**PO-2**	**PO-3**	**PO-4**	**PO-5**	**PO-6**	**PSO-1**	**PSO-2**
CO-1	3	2	-	-	-	-	3	-
CO-2	2	3	-	-	-	-	3	-
CO-3	3	3	-	2	-	-	3	2
CO-4	2	2	-	-	-	-	2	-

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Introduction: Need for Low Power VLSI Chips, Sources of Power Dissipation, Dynamic Dissipation in CMOS, Short Circuit Current in CMOS, CMOS Leakage Current, Basic Principles of Low Power Design, Transistor Sizing & Gate Oxide Thickness, Impact of Technology Scaling, Technology & Device Innovation. Simulation Power analysis: SPICE circuit simulators, gate-level logic simulation, capacitive power estimation, static state power, gate-level capacitance estimation, architecture-level analysis, Monte Carlo simulation.	09
Module-II	Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. Low Power Circuit's: Transistor and gate sizing, network restructuring and Reorganization. Special Flip Flops & Latches design, high capacitance nodes, low power digital cells library. 44	09
Module-III	Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. Low power	09

	Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components.	
Module-IV	Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. Special Techniques: Power Reduction in Clock networks, CMOS Floating Node, Low Power Bus Delay balancing, and Low Power Techniques for SRAM.	09

Learning Resources:

Textbooks:	1. Kaushik Roy, Sharat Prasad, Low-Power CMOS VLSI Circuit Design, Wiley, 2000 2. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP, 2002
Reference Books:	1. Rabaey, Pedram, Low power design methodologies, Kluwer Academic, 1997

Course Title:	**MAPPING SIGNAL PROCESSING ALGORITHMS ON DSP ARCHITECTURES**
Course Code:	**ECVM 571**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Digital Signal Processing (DSP)**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Examine efficient DSP computing algorithms like FFT and Goertzel for optimized signal processing on digital systems.	Remember (Level I)
CO-2	Analyze the impact of C language extensions on DSP architectures and development workflows using simulation and debugging tools.	Understand (Level II)
CO-3	Apply DSP architectures based on benchmarking metrics such as MIPS, power, and code density using real-world architecture comparisons.	Apply (Level III)
CO-4	Evaluate inter-processor communication, firmware partitioning, and hardware-software trade-offs in modern DSP systems and emerging trends.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:

Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Digital systems, DSP, computer architecture, DSP computing algorithms, Direct Computing DFT, FFT, Gortzel.	09
Module-II	Digital systems, DSP, computer architecture, DSP development platforms, C compiler, Impact of C on architecture and vice versa, Extensions to C, DSP-C, Simulation Technologies, program verification, Debug and emulation.	09
Module-III	Benchmarking, MIPS, BDTi, EEMBC, More than MIPS: power, code density, Impact of architecture on performance, Comparison of example architectures (ADI, Philips R.E.A.L., TI C55/C6x).	09
Module-IV	Inter-processor communication, Communication channels, Firmware partitioning problems, Debug and Emulation concepts. Trend: towards higher performance. Trend: merge microcontrollers with DSPs. Trend: time-to-market: do we need floating point, C hardware.	09

Learning Resources:

Text Books:	1. J.G. Ackenhausen, Real-Time Signal Processing Design and Implementation of Signal Processing Systems, IEEE Press Prentice Hall, 2000. 2. V.K.Madisetti, VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis, IEEE Press Butterworth-Heinemann, 1998 3. J. Proakis, D. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Fourth edition, 2006, Prentice-Hall.
Reference Books:	1. K.J.Ray Liu and K.Yao, High Performance VLSI Signal Processing: Systems Design and application, Vol. 2, 1998, IEEE Press.

Course Title:	**MOS DEVICES MODELLING AND CHARACTERIZATION**
Course Code:	**ECVM 572**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Basic Electronics / Devices & Circuits**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Assess the energy band diagram and 1D electrostatics of MOS structures under various operating modes.	Remember (Level I)
CO-2	Analyze CV characteristics of MOS capacitors considering threshold voltage behavior and non-ideal effects such as oxide and interfacial charges.	Understand (Level II)
CO-3	Apply MOSFET current-voltage models to analyze device behavior in weak, moderate, and strong inversion, including effects of body bias, series resistance, and temperature.	Apply (Level III)
CO-4	Evaluate the impact of short-channel effects, velocity saturation, hot-carrier effects, quantum mechanical effects, and scaling challenges on modern MOSFET performance.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.	09
Module-II	CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges. Threshold voltage capacitance voltage relation, The three terminal MOS structure, effect of body bias on surface conditions, Threshold voltage with body bias.	09
Module-III	The four terminal Metal Oxide Semiconductor transistor, strong inversion, moderate inversion and weak inversion current, voltage models, Effective mobility, Effect of source and drain series resistance, Temperature effects, Break down.	09
Module-IV	Ebers-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics. Short channel and thin oxide effects, carrier velocity saturation, channel length modulation, charge sharing, Drain Induced barrier lowering, punch through, Hot carrier effects, Impact ionization, Velocity overshoot, Ballistic operation, Quantum Mechanical effects, DC gate current, Junction leakage, Band to band tunneling, Gate Induced Drain Leakage (GIDL), MOSFET scaling	09

Learning Resources:

Text Books:	1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981. 2. Yuan Taur&Tak H Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 2013. 3. Y. Tsividis& Colin McAndrew, The MOS Transistor, 3rd Edition, Oxford University Press, 2013.
Reference Books:	1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987. 2. E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.

Course Title:	**MIXED SIGNAL IC DESIGN**
Course Code:	**ECVM 573**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Analog Electronics / Analog Circuits**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Design and analyze fundamental analog building blocks such as current mirrors, amplifiers, and differential pairs in CMOS technologies.	Remember (Level I)
CO-2	Analyze non-idealities in sampling systems and evaluate performance metrics of switched-capacitor circuits and data converters.	Understand (Level II)
CO-3	Apply various ADC and DAC architectures with respect to noise, linearity, jitter, and signal-to-noise ratio (SNR) to choose optimal converters for applications.	Apply (Level III)
CO-4	Evaluate noise-shaping techniques and topology selection in designing high-speed, high-resolution data converters for analog/mixed-signal systems.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:		
Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Introduction to analog VLSI and mixed signal issues in CMOS Technologies, MOS transistor: Introduction, Short channel effects, current source and current mirror, Common-Source Amplifier, Source-Follower, Source Degenerated Current Mirrors, cascode Current Mirrors, MOS Differential Pair and Gain Stage, active load, C- MOS circuit.	09
Module-II	Ideal Sampling, Non idealities in sampling, noise and distortion in sampling, sample and hold circuits, timing issues in sample and hold circuit, bootstrapping systems, charge injection and noise, introduction to switched capacitor circuits, switched capacitor sample and hold circuits, static specifications of data converters, accuracy, nonlinearity, offset, dynamic specifications, SNR, SFDR, ENOB, dynamic range.	09
Module-III	D/A and A/D converters: Introduction A/D and D/A, Various type of A/D converter, ADCs, ramp, tracking, dual slope, successive approximation and flash types, Multi-stage flash type ADCs, Signal-to-Noise Ratio (SNR), Clock Jitter and A Tool: The Spectral Density, Improving SNR using Averaging, Linearity	09

	Requirements, Adding a Noise Dither, Jitter, and Anti-Aliasing Filter, Using Feedback to Improve SNR. Passive Noise-Shaping - Signal-to-Noise Ratio and Decimating and Filtering the Modulator's Output, Offset, Matching, and Linearity. Improving SNR and Linearity - Second-Order Passive Noise-Shaping and Passive, Noise-Shaping Using Switched-Capacitors, Increasing SNR using K-Paths and Improving Linearity Using an Active Circuit.	
Module-IV	First-Order Noise Shaping - Modulation Noise in First-Order NS Modulators, RMS Quantization Noise in a First-Order Modulator, and Decimating and Filtering the Output of a NS Modulator, Pattern Noise from DC Inputs (Limit Cycle Oscillations), Integrator and Forward Modulator Gain, Comparator Gain, Offset, Noise, and Hysteresis, and, Op-Amp Gain (Integrator Leakage) Op-Amp: Settling Time, Offset, Op-Amp Input-Referred Noise, and Practical Implementation of the First-Order NS Modulator, Second–Order Noise Shaping, Second–Order Modulator Topology, Integrator Gain, and Selecting Modulator (Integrator) Gains. Noise–Shaping Topologies – Higher–Order Modulators, Filtering the Output of an M^{th}–Order NS Modulator, Implementing Higher–Order, Single–Stage Modulators, Multi–Bit Modulators, and Error Feedback Continuous–Time Band pass Noise–Shaping – Passive–Component Band pass Modulators, Active–Component Band pass Modulators, and Modulators for Conversion at Radio Frequencies, Cascaded Modulators, Switched Capacitor Band pass Noise–Shaping – Switched–Capacitor Resonators, Second Order Modulators, Fourth–Order Modulators, and Digital I/Q Extraction to Baseband, Topology of a high–speed data converter – Clock Signals, Implementation, Filtering, Discussion, and Understanding the Clock Signals.	09

Learning Resources:

Text Books:	1. Baker, R. Jacob, "CMOS: mixed-signal circuit design", john Wiley &Sons, 2008. 2. R. Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, 2nd Edition, Springer, 2007.
Reference Books:	1. R. Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", 2nd Edition, Springer, 2007 2. M. J. M. Pelgrom, "Analog-to-Digital Conversion", Springer, 2010

Course Title:	**HIGH SPEED SYSTEM DESIGN (BOARD LEVEL)**
Course Code:	**ECVM 574**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Signals and Systems / DSP/Analog Circuits / Electronic Devices**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	Examine the impact of crosstalk, non-ideal return paths, and simultaneous switching noise on signal integrity in high-speed digital systems.	Remember (Level I)
CO-2	Analyze PCB design techniques, fabrication processes, and thermal management strategies for reliable high-speed circuit operation.	Understand (Level II)
CO-3	Apply PCB design techniques, fabrication processes, and thermal management strategies for reliable high-speed circuit operation.	Apply (Level III)
CO-4	Evaluate interconnect modeling techniques and testing methodologies to mitigate EMI and ensure performance in high-speed systems.	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:

Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Crosstalk and non-ideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high-speed buses; radiated emissions and minimizing system noise; Practical aspects of measurement at high frequencies; high speed oscilloscopes and logic analyzers.	09
Module-II	Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation Cooling requirements.	09
Module-III	Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging, reliability, wafer level burn – in and test. Single chip packaging: functions, types, materials processes, properties, characteristics, trends. Multi-chip packaging: types, design, comparison, trends. Passives: discrete, integrated, embedded – encapsulation and sealing:	09

	fundamentals, requirements, materials, processes.	
Module-IV	Interconnect Capacitance, Resistance and Inductance fundamentals; Transmission Lines, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI, Digital and RF Issues. Processing Technologies, Thin Film deposition, Patterning, Metal to Metal joining. Basic concepts, Environmental interactions. Thermal mismatch and fatigue failures thermo mechanically induced electrically induced chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.	09

Learning Resources:

Text Books:	1. Tummala, Rao R., "Fundamentals of Microsystems Packaging", McGraw Hill, 2001 2. Howard Johnson, Martin Graham, "High Speed Digital Design: A Handbook of Black Magic", Prentice Hall, 1993 3. Stephen H. Hall, Garrett W. Hall, James A. McCal , "High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices", Wiley-IEEE Press, 2000
Reference Books:	1. Tummala, Rao R, "Microelectronics packaging handbook", McGraw Hill, 2008. 2. Bosshart, "Printed Circuit Boards Design and Technology", Tata McGraw Hill, 1988.

Course Title:	**ADVANCED DIGITAL SYSTEM DESIGN**
Course Code:	**ECVM 575**
L-T-P:	**3-0-0**
Credits:	**3**
Pre-requisites:	**Digital Logic Design / Digital Circuits**

Course Outcomes:

Course Outcomes:		**Cognitive Levels**
CO-1	To design and analyze Synchronous and Asynchronous sequential logic circuits	Remember (Level I)
CO-2	To understands, realize and design hazard free circuits.	Understand (Level II)
CO-3	To acquire the knowledge about different fault diagnosis and testing methods	Apply (Level III)
CO-4	To evaluate the design approaches using PLDs and various FPGAs	Evaluate (Level V)

Course Articulation Matrix:

	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PSO-1	PSO-2
CO-1	3	1	2	1			2	
CO-2	3	2	1	1			2	
CO-3	3	1	2	1			2	
CO-4	2	3	1	1			2	

1 - Slightly; 2 - Moderately; 3 - Substantially

Syllabus:

Module	**Detailed Syllabus**	**Contact Hours**
Module-I	Synchronous Sequential Circuit Design: Introduction, Moore, Mealy and Mixed Type Synchronous State Machines. Analysis of clocked synchronous sequential circuits and modeling, state diagram, state table, state table assignment and reduction, design of synchronous sequential circuits, design of iterative circuits, ASM chart and realization using ASM.	09
Module-II	Asynchronous Sequential Circuit design: Introduction, Analysis of asynchronous sequential circuit (ASC), Primitive flow table and reduction, type of delays, Cycles and races, state assignment problems and transition table, Excitation Map, Design of ASC, Statics and Dynamic Hazards, Essential hazards. Design vending machine controller, Mixed operating mode asynchronous circuits.	09
Module-III	Fault Diagnosis and Testability Algorithms: Fault table method, Path sensitization method, Boolean difference method, D-Algorithms, Tolerance techniques, The compact algorithms, Practical PLA's, Fault in PLAs, Test Generation, Masking Cycles, DFT Schemes, Built in self-test.	09
Module-IV	Design using Programmable Logic Devices: Programming logic device families, designing of synchronous sequential circuits using PLA/PAL, Realization of finite state machines using PLD, Designing with FPGAs, Xilinx FPGA.	09

Learning Resources:

Text Books:	1. Donald D.Givone, "Digital Principles and Design", McGraw Hill, 2nd edition 2. Shanthi, A. Kavitha, A., Martin Graham, "VLSI Design", New Age International, 2nd Edition 3. Uyemura, John P., "CMOS Logic Circuit Design", Springer 2nd Edition
Reference Books:	1. M.Morris Mano, "Digital Design", Pearson Education, 3rd edition, 2. Charles H.Roth, Jr, "Fundamentals of Logic Design", Jaico Publishing House, 4th Edition. 3. Michael D.Ciletti, "Advanced Digital Design with the Verilog HDL", Pearson Education, 2nd edition